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DEVELOPMENT OF SPECTRAL ANALYSIS MATH MODELS  
AND SOFTWARE PROGRAM AND SPECTRAL ANALYZER -  
DIGITAL CONVERTER INTERFACE EQUIPMENT DESIGN

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FINAL REPORT

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**TRW**  
SYSTEMS GROUP

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## 1. INTRODUCTION AND SUMMARY

This final project report presents the results of a one year contract to provide NASA/MSC with the capability of performing spectral analyses of angle modulated communication systems. The contract was conducted in three phases by 1) performing a literature survey of candidate power spectrum computational techniques, determining the computational requirements, and formulating a mathematical model satisfying these requirements, 2) implementing the model on the Electronic Systems Test Laboratory (ESTL) UNIVAC 1230 digital computer as the Spectral Analysis Program (SAP), and 3) developing preliminary hardware specifications for a data acquisition system which will acquire an input modulating signal for SAP.

The computation of the power spectrum for a communication system in which the phase or frequency of a high-frequency carrier wave is modulated by a complex signal poses a difficult and/or time consuming problem, even when performed by a high-speed digital computer. This difficulty stems from several sources. First, many modulating signals of practical interest include high frequency components. In this case, the number of data samples required to represent the modulating signal according to the Nyquist sampling theorem may be large. Secondly, the inherent non-linearity of the angle modulation process precludes the simplified analysis usually resulting from application of the superposition principle. Instead of a closed-form solution based on the superposition principle, a series representation of the solution is required. The series representation computation is especially time consuming when a large number of data samples must be processed. The non-linearity theoretically generates an infinite number of new frequency components. Although theoretically infinite, the number of components with significant magnitudes is limited to a finite number. In general, however, the angle modulated spectrum is significantly broader than the original baseband spectrum, the spectral extent increasing as the modulation index increases. Consequently, the number of samples required to represent

the modulated signal may be very large. Thirdly, power spectrum computations require one or more Fourier (or Fourier-like) transformations between the time and frequency domains. The Fourier transform of  $N$  data samples involves multiplying an  $N \times 1$  column matrix by an  $N \times N$  Fourier matrix operator (with complex matrix elements). This multiplication is very time consuming for large  $N$ . Finally, the evaluation of an angle modulation communication system often involves low pass filtering the modulating signal and/or band-pass filtering the modulated signal. If the filtering computation is performed in the time domain, the signal must be convolved with the unit impulse response of the filter; if the filtering is performed in the frequency domain, the signal is transformed to the frequency domain and then multiplied by the filter transfer function. In either case, the filtering computation time may be excessively lengthy for many signals of practical interest.

A computational technique which greatly reduces the power spectrum computation time and is applicable to complex modulating signals has been formulated and implemented on the UNIVAC 1230 digital computer. The technique is based on the Fourier transform approach, but uses the fast Fourier transform (FFT). Since its appearance in technical literature during the past few years, the FFT has revolutionized digital signal processing. The FFT now permits the transformation between the frequency and time domains with reasonable computational economy. For example, an FFT of 16,384 data samples uses a factor of about 1/2000 fewer multiply-add operations than the non-FFT.

A noteworthy contract achievement was development of the extended fast Fourier transform (EFFT). The EFFT provides capability for Fourier transforming data arrays much larger than the available computer core memory. The EFFT technique divides a large data array into sub-arrays, performs the FFT of each sub-array and stores the results on magnetic tape. The resulting transforms are then appropriately combined to simulate the Fourier transform of the large data array. Both spectral analysis and digital filtering computational capabilities on the ESTL UNIVAC 1230 computer are greatly extended using the EFFT.

The power spectrum computational model was implemented as the Spectral Analysis Program (SAP). SAP either accepts an externally supplied modulating signal existing on tape, or internally generates a sum of sinusoids signal, a periodic square wave, or a periodic multilevel signal. After acceptance or generation, the input modulating signal may be low-pass filtered using either a Butterworth, Chebyshev, or user defined filter. The signal is then multiplied by the modulation parameter and exponentiated to simulate the modulation process. Next, the modulated signal may be bandpass filtered using the same filters mentioned above. Finally, the power spectrum is computed and printed. The power spectrum is also stored on a magnetic tape (called the SAP plot tape).

A user's guide for SAP has been prepared and is presented in Reference 1 (Spectral Analysis Program, Volume I - User's Guide). The purpose of the guide is to provide the user with the necessary information to 1) understand the general computational approach, 2) set-up the input parameters in the appropriate card or tape format, and 3) execute the program. A programmer's manual, containing the software flow diagrams and listings, is presented in Reference 2 (Spectral Analysis Program, Volume II - Programmer's Manual).

The Plot Generation Program (PLTGEN) was designed and implemented on the UNIVAC 1230. PLTGEN accepts the SAP plot tape, converts the spectral data into plot commands for the EAI 3440 Dataplotter, and writes these commands on magnetic tape. This tape then drives the Dataplotter and generates a power spectrum plot.

The preliminary hardware specifications for a data acquisition system for the UNIVAC 1230 computer was developed. The system accepts a wideband analog signal, performs periodic sampling at a specified sampling rate, converts each sample to a digital format, and supplies the resulting digital samples to the computer at a rate and in a form compatible with the computer functional and electrical design characteristics. Although designed specifically to acquire a modulating signal for the Spectral Analysis Program, the hardware design is flexible enough to function as a general purpose wideband data acquisition tool.

## 2. TECHNICAL DISCUSSION

The technical discussion is presented in three sections, corresponding to the three phases of the contract. Section 2.1 describes the basic analytical problem, candidate power spectrum computational approaches, and the selected approach. A detailed theoretical analysis of the computational model and limitations is presented. Section 2.2 describes the software implementation of the model on the ESTL UNIVAC 1230 computer and presents verification results. Section 2.3 describes the hardware design of a data acquisition system which acquires digital samples of the modulating signal for input to the software program.

### 2.1 MATHEMATICAL FORMULATION

#### 2.1.1 Basic Analytical Problem

The basic analytical problem is the development of a power spectrum computational model which simulates the angle modulation system and display shown in the block diagram of Figure 2-1. The model contains a signal source representing the input modulating signal, capability for lowpass filtering the modulating signal, a modulator which exponentially modulates the modulating signal onto a high frequency carrier, capability for bandpass filtering the modulated signal, and the computation/display of the power spectrum.

The modulated signal  $v(t)$  generated by the process of angle modulation may be written

$$v(t) = \cos[\omega_c t + \beta \phi(t)] \quad (1)$$

where  $\phi(t)$  represents a time varying phase function  $g(t)$  normalized to unit peak amplitude, i.e.,

$$\phi(t) = \frac{g(t)}{|g(t)|_{\max}} \quad , \quad |\phi(t)| \leq 1. \quad (2)$$



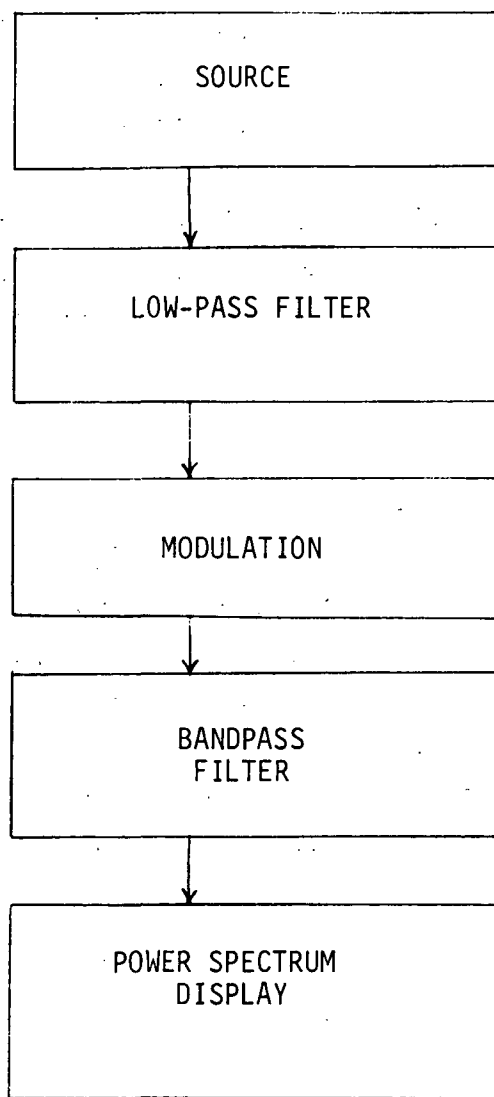
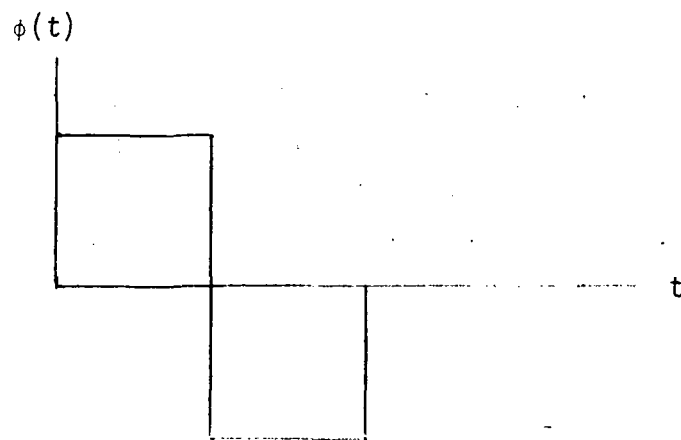
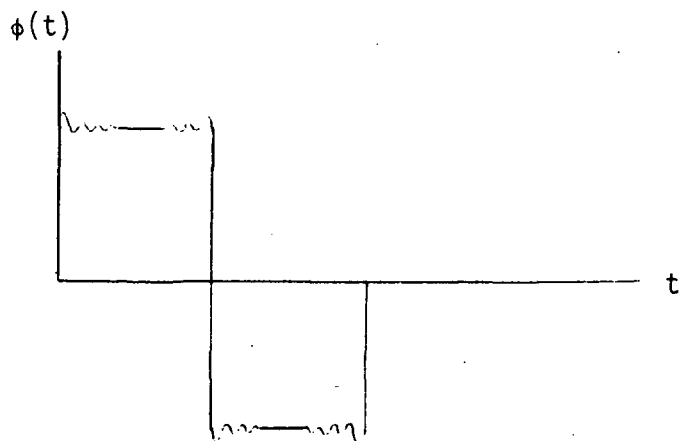


Figure 2-1. Angle Modulation System and Power Spectrum Display



(a) True Square Wave Modulating Signal



(b) Approximate Square Wave Modulating Signal

Figure 2-10. Gibbs Phenomenon

increased further, the ripples show a proportionately increased rate of oscillation, but the ripple amplitudes relative to the magnitude of the discontinuity remains the same. As  $n \rightarrow \infty$ , the ripples are compressed into a single vertical line at the point of discontinuity. The square wave can never be approximated in the vicinity of the discontinuity with an error less than 18 percent.

## 2.2 SOFTWARE IMPLEMENTATION

### 2.2.1 The Spectral Analysis Program

The Spectral Analysis Program (SAP) computes the power spectrum of an angle modulated high frequency carrier wave. The program is designed to 1) provide capability for performing spectral analyses of a wide variety of angle modulated signals likely to be encountered in the testing and evaluation of angle modulated communication systems, 2) be operationally compatible with the Electronic Systems Test Laboratory (ESTL) UNIVAC 1230 digital computer, and 3) generate a power spectrum data tape compatible with the Plot Generation Program (PLTGEN). PLTGEN generates the appropriate commands to drive the EAI 3440 Dataplotter and create the power spectrum plot.

A simplified block diagram of SAP is presented in Figure 2-11. SAP either accepts an externally supplied modulating signal existing on magnetic tape or internally generates a user specified modulating test signal. The user specified signal may be selected from 1) a sum of sinusoids containing up to 25 frequency components (the amplified, phase, and frequency of each component are user specified), 2) a periodic five level signal in which the incremental amplitude levels and switching times are specified, and 3) a periodic square wave in which the amplitude and period are specified. After acceptance or generation, the input modulating signal may be low-pass filtered using either a Butterworth, Chebyshev, or user defined filter. For the Butterworth and Chebyshev filters, the user selects the filter order, cut-off frequency, and the amount of ripple (Chebyshev filter only). For the user defined filter, the filter transfer function is defined by the linear interpolation of the magnitude and phase for up to 50 frequency break-points supplied by the user. After low-pass filtering, the modulating signal is multiplied by the modulation parameter and then exponentiated to simulate the exponential modulation process. Next, the modulated signal may be band-pass filtered, using the same filters mentioned above. In addition, the bandpass center frequency may be specified. Finally, the power spectrum is computed, two output tapes are generated, and the output spectrum is printed.

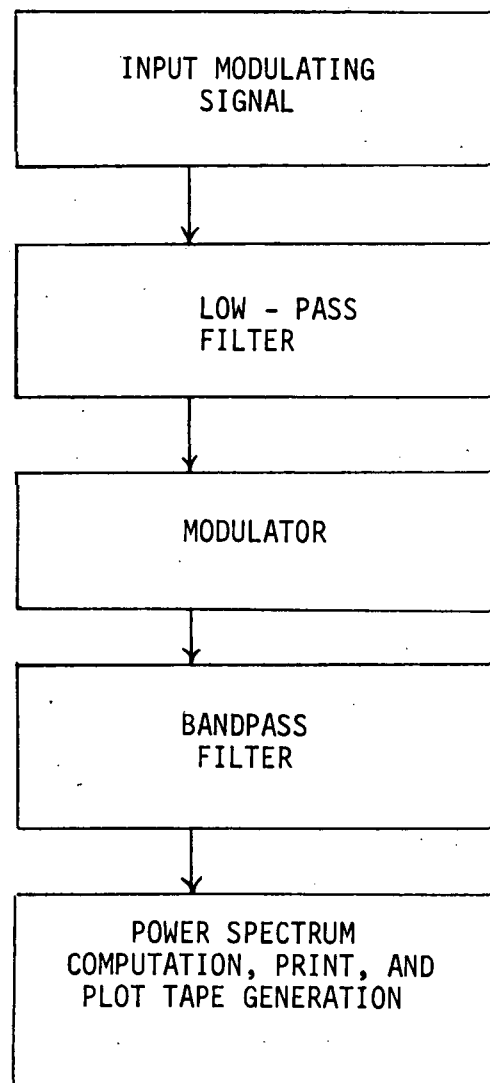


Figure 2-11. SAP Simplified Block Diagram

As stated above, two output tapes are available at the conclusion of a SAP execution. The first tape is called the SAP plot tape and is used as input to PLTGEN. PLTGEN, in turn, generates another tape which is mounted on the EAI plotter unit and drives the plotting pen. The second tape is called the SAP spectrum tape and contains the Fourier transform of the modulated signal. This tape is re-input to SAP after the first SAP execution when displays of additional spectral regions are desired, as discussed below.

The computed power spectrum may contain up to 16,384 spectral lines at a frequency resolution  $\Delta f = \frac{1}{16,384 \Delta t}$ , where  $\Delta t$  is the sampling interval in seconds. If desired, a specified number of adjacent spectral lines of the computed spectrum may be averaged to provide a power spectrum of lower resolution.

SAP is implemented based on the modular software design concept. The modules closely resemble the physical process being simulated. The input signal for a given module resides on one of two magnetic tapes; the output signal is computed and stored on the second tape. The second (output) tape then functions as the input tape for the next module; i.e., the program switches the tape unit labels for both tapes.

The points in the driver program at which tape unit label switching occurs are called entry points. Ten entry points exist and are labeled 100, 200, 300, 400, 500, 600, 700, 800, 900, and 1000 on the output listing. As each entry point is passed during program execution, the following messages are printed:

```
PROGRAM HAS PASSED ENTRY POINT XXXX.  
DATA IS CURRENTLY ON UNIT XI.  
SPARE TAPE IS CURRENTLY ON UNIT X2.  
THERE ARE X ROWS AND Y COLUMNS OF DATA.  
EXECUTION TIME = X MINUTES, Y SECONDS.
```

The modular software design provides a convenient recovery capability should a machine or other failure occur. To recover after a failure, the user specifies the last entry point passed, the data unit number, and spare tape unit number as provided by the last set of entry point messages. The driver program then jumps to the specified entry point and execution of SAP continues. (Note: the entry points are labeled 100, 200, 300, 400, 500, 600, 700, 800, 900, and 1000 on the output listing; to re-execute SAP, the input entry points are 1, 2, 3, 4, 5, 6, 7, 8, 9, and 10, respectively.)

Several power spectrum print and plot display options are available to provide maximum display utility to the user. Each point or plot may contain up to 480 spectral lines (corresponding to a maximum plot resolution of 20 lines per inch). In the carrier centered display, the carrier is centered along the frequency axis and the spectral region associated with 240 lines to the left of the carrier and 240 lines to the right of the carrier is displayed. In other displays, the starting frequency is user specified and the spectral region associated with the starting frequency plus the next 479 lines is displayed. Spectral regions larger than 480 lines may be displayed by additional plots in which the starting frequency is the last frequency of the previous plot. The entire SAP program need not be re-executed in this case; only the last part of the program (from entry point number 10) is re-executed. Thirty-five plots are required to display the maximum size computed spectrum of 16,384 lines.

All parameters describing the plot are input to SAP; PLTGEN does not require any user controlled input parameters.

### 2.2.2 Functional Flow Diagram

The Spectral Analysis Program functional flow diagram is presented in Figure 2-12. All modules or subroutines developed are shown. Brief descriptions of each module or subroutine are presented below:

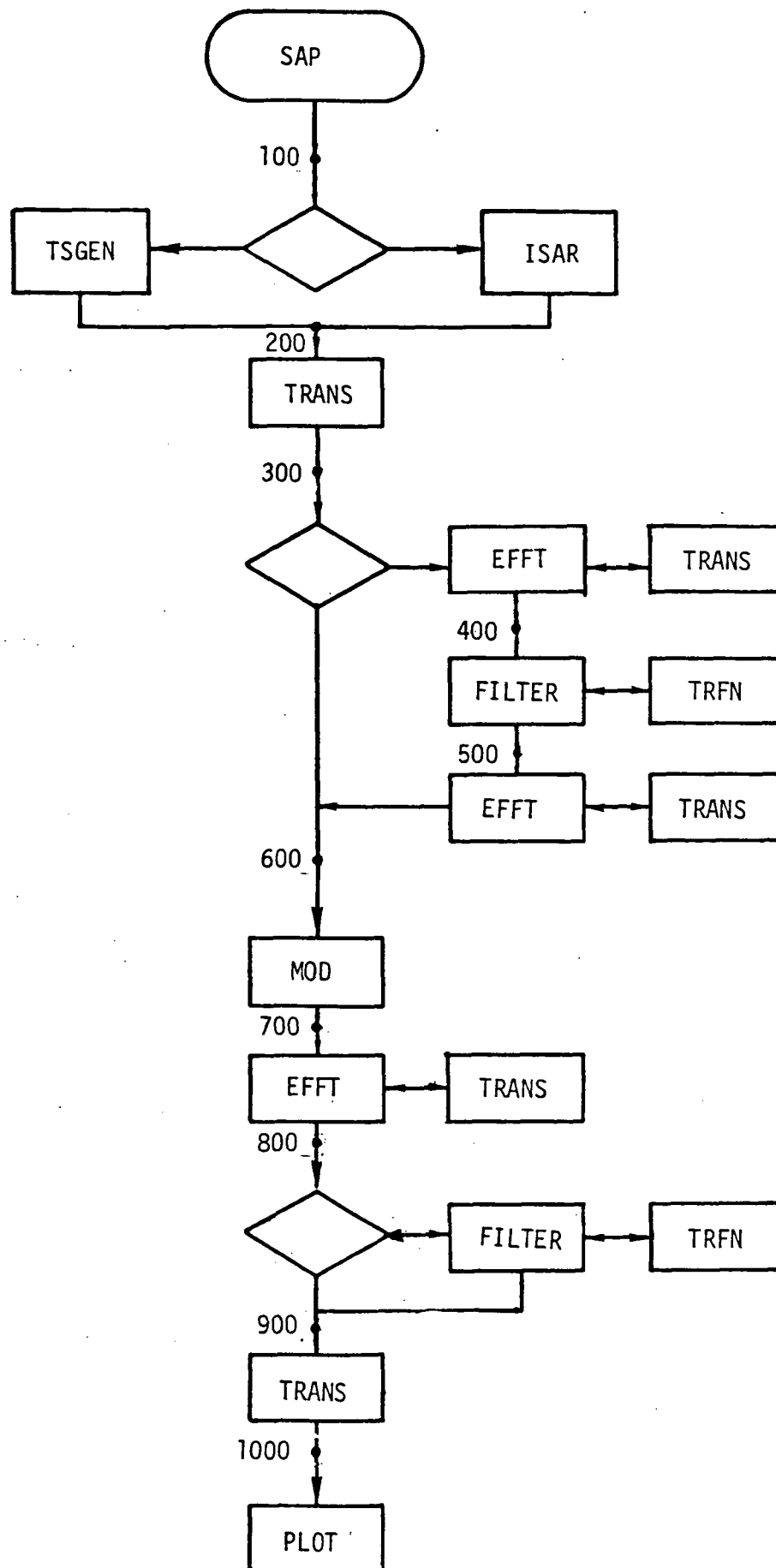


Figure 2-12. Spectral Analysis Program Functional Block Diagram



- SAP - Driver for Spectral Analysis Program.
- TSGEN - Computes the internally generated test signals  $\phi(t_k)$ . These signals are: 1) sum of sinusoids, 2) periodic multilevel, and 3) square wave. (Refer to Section 2.1.3.3)
- ISAR - Accepts and resamples input modulating signal. (Refer to Section 2.1.3.3)
- EFFT - Computes the extended fast Fourier transfer. (Refer to Appendix A)
- TRANS - Transposes the signal array as required by EFFT. (Refer to Appendix A)
- FILTER - Filters the modulating and/or modulated signals; i.e., multiplies the Fourier transform of the modulating or modulated signal by the filter transfer function. Also, integrates the modulating signal for frequency modulation. (Refer to Section 2.1.3.2)
- TRFN - Computes the filter transfer function for the Butterworth, Chebyshev, and user filters. (Refer to Section 2.1.3.2)
- MOD - Computer  $e^{-j\beta\phi(t)}$ . (Refer to Section 2.1.1)
- PLOT - Computes the power spectrum, generates SAP plot tape and SAP sepctrum tape, and prints spectrum. (Refer to Section 2.1.1)

### 2.2.3 Input Parameters

The input parameters and options for the Spectral Analysis Program are presented in Table 2-3.

### 2.2.4 Limitations

This section lists SAP operational constraints.

- . The total number of data samples  $N = NCIDT * NRIDT$  must not exceed 16,384. NCIDT is the number of columns of data and NRIDT is the number of rows of data.

Table 2-3. Inputs for Spectral Analysis Program

General

IEP	- defines entry point to the driver by
	= $\begin{cases} 1 - \text{nominal run} \\ K - \text{restart entry point} \end{cases}$
IDT IST	- defines data tape and spare tape units. For normal cases, IDT = 1 and IST = 2. For restart capability (IEP $\neq$ 1), signal data resides on IDT.
NCIDT NRIDT	- defines the number of points, N, in the test signal by $N = \text{NCIDT} * \text{NRIDT}$ . Each <u>must</u> be a power of 2. For efficiency, NCIDT and NRIDT should be approximately equal (for example NCIDT = 64 and NRIDT = 128). For restarting (IEP $\neq$ 1), NCIDT and NRIDT define the number of columns and rows, respectively, of the arrays on tape IDT.
ISOPT	- defines signal option by
	= $\begin{cases} 0, \text{user input signal on tape IDT} \\ 1, \text{sinusoidal test signal} \\ 2, \text{periodic four level gray test signal} \\ 3, \text{periodic square wave test signal} \end{cases}$
IFM	- defines modulation type by
	= $\begin{cases} 1, \text{FM modulation} \\ 2, \text{phase modulation} \end{cases}$
IFOPT	- defines filtering options
	= $\begin{cases} 0, \text{no filtering} \\ 1, \text{filter modulating signal only} \\ 2, \text{filter modulated signal only} \\ 3, \text{filter modulating and modulated signal} \end{cases}$

Table 2-3. Inputs for Spectral Analysis Program (Continued)

BETA	- defines modulation index by
=	$\begin{cases} \text{if IFM} = 1, \text{ BETA} = \text{maximum frequency deviation (Hertz)} \\ \text{if IFM} = 2, \text{ BETA} = \text{maximum phase deviation (radians)} \end{cases}$
DELT	= time separation (in seconds) between points in test signal or between user input signal prior to resampling
FC	= carrier frequency (in Hertz)
IZPRT(I)	- special print control
	0, no special print
=	1, special print at indicated entry point
<u>I</u>	<u>ENTRY POINT</u>
1	2
2	4
3	5
4	6
5	8
6	9

### Test Signals

#### a) Sinusoids (ISOPT = 1)

M - number of sinusoids ( $\leq 25$ )

A(I) - amplitude of  $I^{\text{th}}$  sinusoid

F(I) - frequency (in Hertz) of  $I^{\text{th}}$  sinusoid

THETA(I) - phase angle (in degrees) of  $I^{\text{th}}$  sinusoid

For IFM = 1, A(I) is the peak frequency deviation associated with each sinusoid

For IFM = 2, A(I) is the peak phase deviation associated with each sinusoid

Note: If ISOPT = 1, the input specification for BETA must be omitted

Table 2-3. Inputs for Spectral Analysis Program (Continued)

b) Periodic four level gray (ISOPT =2)

TP(I) - I = 1, 2, 3, 4 - defines the time points (in seconds)  
of the breaks or changes in the signal

A(I) - I = 1, 2, 3, 4 - defines the corresponding changes in  
the amplitude of the signal

TP(5) - defines period of signal

c) Periodic Square Wave (ISOPT = 3)

TP(1) - period (in seconds) of the square wave

A(1) - amplitude of square wave

Input Signal

NR1 - number of words per record on input data tape

NC1 - number of records on input data tape

KSR - defines sampling rate for resampled signal by DELT/KSR

Filtering (depending on IFOPT - zero, one or two filters need to be  
specified)

a) for the modulating signal

IFTYP1 - defines filter type by

$$= \begin{cases} 1, & \text{Butterworth} \\ 2, & \text{Chebychev} \\ 3, & \text{Input filter} \end{cases}$$

NORD1 - defines order of Butterworth or Chebychev filter  
( $\leq 5$ )

FCUT1 - defines cutoff frequency of Butterworth or Chebychev  
filter (in Hertz)

RIP1 - defines ripple for Chebychev filter

Table 2-3. Inputs for Spectral Analysis Program (Continued)

- NF1 - for IFTYP1 = 3, defines number of points specified for input filter ( $\leq 50$ )
- TMAG1(I) - for IFTYP1 = 3, defines magnitude of input filter transfer function at I<sup>th</sup> frequency
- TPH1(I) - for IFTYP1 = 3, defines corresponding phase (in radians) at I<sup>th</sup> frequency
- F1(I) - for IFTYP1 = 3, defines frequency (in Hertz) at which magnitude and phase is specified
- intermediate values of the magnitude and phase are generated by using linear interpolation over the input values

b) for the modulated signal

IFTYP2	} identical in definition as corresponding variables for modulating or test signal filter - but apply to filtering the modulated signal. The additional parameter FCEN2 defines the center frequency for the bandpass filter.
NORD2	
FCEN2	
FCUT2	
RIP2	
NF2	
TMAG2(I)	
TPH2(I)	
F2(I)	

### Plot

- FSTRT - frequency (in Hertz) at which plot display begins; if  $< 0$ , then display with centered FC is generated.
- AMAX - scaling factor in output plot, if set to zero the plot module computes AMAX as maximum power component in total signal and scales data to be plotted by this value, if set positive then the input value is used to scale data for plotting.
- NAVE - number of points to be averaged for each output display point, each output point represents a bandwidth of  $\text{NAVE} \cdot \Delta f$  where  $\Delta f = 1/(\text{NRIDT} \cdot \text{NCIDT} \cdot \text{DELT})$

Table 2-3. Inputs for Spectral Analysis Program (Continued)

IPMODE	- controls printing and plotting by = { 0, print and plot 1, plot only 2, print only
IPLPOS	- controls plot position on page by = { 0, top half 1, bottom half
ITITLE	- 30 characters for title on run and title on plot

- . The total number of data samples  $N = \text{NCIDT} * \text{NRIDT}$  must be an integral power of two; i.e.,  $N = 2^n$ , where  $n = 1, 2, 3, \dots, 13, 14$ .
- . The maximum value of NCIDT or NRIDT is 256. (For example, if  $N = 16,384$ , the following factors are acceptable:  $N = \text{NCIDT} * \text{NRIDT} = 256 * 64, 128 * 128$ , and  $64 * 256$ . If  $N = 4096$ ,  $N = 256 * 16, 128 * 32, 64 * 64, 32 * 128$ , and  $16 * 256$ .)
- . The sum of sinusoids modulating signal generated internally must contain 25 or fewer sine wave components; i.e.,  $M \leq 25$ .
- . Use of the Butterworth filter is restricted to filter orders one through six; i.e., NORD1 or NORD2 = 1, 2, 3, 4, 5 and 6. NORD1 and NORD2 are the filter orders of the low-pass and bandpass filters, respectively.
- . Use of the Chebyshev filter is restricted to filter orders one, three, and five; i.e., NORD1 or NORD2 = 1, 3, and 5. Even order Chebyshev filters are generally physically unrealizable for equal source and load impedances.
- . Use of the user filter is restricted to 50 break-points; i.e., NF1 or NF2  $\leq 50$ . NF1 and NR2 are the number of frequency break-points for the low-pass and bandpass filters, respectively.

#### 2.2.5 Verification

The Spectral Analysis Program was verified at the individual module level and at the overall software package level. Verification was accomplished using test cases with known theoretical results. For example, at the overall software package level, the computed power spectrum was compared with theoretical results for phase and frequency modulating signals consisting of sine waves and periodic square waves. Results indicated a minimum of six significant figures accuracy for the power spectrum expressed in decibels.

This high degree of accuracy is a direct result of using the EFFT technique to compute the Fourier transforms. Use of the EFFT for complex modulating signals is advantageous because 1) the number of multiply-add operations

is reduced significantly compared to non-FFT power spectrum computational techniques and 2) the EFFT optimally accumulates a long series of floating point numbers. The optimal accumulation method is to add pairs of numbers, then pairs of the resulting sums, etc. The error generated by the EFFT was investigated experimentally by performing the EFFT of a unit impulse, performing the inverse EFFT, and then examining the difference between the original and reconstructed set of data. At least seven significant figures of agreement, depending on the array size, was obtained.

A sample case is presented to demonstrate the program accuracy, capabilities, and options. The sample case includes specification of the problem, sample coding form, sample listing of the program input and output, and the associated power spectrum plot.

Example. Compute the power spectrum of a 1 MHz carrier ( $FC = 1 \times 10^6$ ) frequency modulated (IFM = 1) by a square wave of frequency 1.5625 Hz (TP = 0.639990) and amplitude unity ( $A = 1.0$ ). Exactly one period of the square wave will be generated internally (ISOPT = 3). A peak frequency deviation of 200 Hz (BETA = 200.0) is desired. No filtering is to be performed. The output power spectrum, centered about the carrier (FSTART = -1.0), is to be both printed and plotted using the maximum available frequency resolution (NAVE = 1). The spectral region of interest is  $1 \times 10^6 \pm 375$  Hz. Based on analytical considerations, the amount of aliasing is estimated to be small in the region of interest if the number of samples is selected to be 1024 (NRIDT = 32 and NCIDT = 32) and the sampling time interval is selected to be  $0.625 \times 10^{-3}$  seconds (DT = 0.000625). (The validity of this estimation may be experimentally verified by comparing with a second power spectrum computation in which the number of samples is doubled and the sampling interval is halved. The estimate is valid when the agreement between the first and second computations is within an acceptable tolerance in the region of interest.)





```

*****
*                                     *
*      *   EXAMPLE 2    MAY 31,1972    *
*                                     *
*****
101 IEP IF-A IFORT IFTYPI IFTYP2 IPLPOS IPMODE ISOPT IST KSR NCIDT NCI NF1 NF2 NRIDT NRI HAVE IZPRY
1 1 1 0 0 0 0 3 2 0 0 32 0 0 0 0 1 0 0 0 0 0
ALUU, BETA = 0.2000000E03, DELT = 0.6250000E-03, FSTART = 0E00, FC = 0.1000000E07
*****
*****
TP A
0.6399999E00 1.0000000E00
*****

```

```

FORM 1411-3
*****
**
** PROGRAM HAS PASSED ENTRY POINT 100.
**
*****

```

```

**      DATA IS CURRENTLY ON UNIT 1.      **
**      SPARE TAPE IS CURRENTLY ON UNIT 2.  **
**      THERE ARE 32 ROWS AND 32 COLUMNS OF DATA.  **
**      EXECUTION TIME = 0 MINUTES, 2.968 SECONDS  **
**      **
*****

```

```

** ***** **
** **
** **
** **
** PROGRAM HAS PASSED ENTRY POINT 200. **
** DATA IS CURRENTLY ON UNIT 1. **
** **
** SPARE TAPE IS CURRENTLY ON UNIT 2. **
** **
** THERE ARE 32 ROWS AND 32 COLUMNS OF DATA. **
** **
** EXECUTION TIME = 0 MINUTES, 4.530 SECONDS **
** **

```

```
*****
**
**
** PROGRAM HAS PASSED ENTRY POINT 300. **
** DATA IS CURRENTLY ON UNIT 1. **
** SPARE TAPE IS CURRENTLY ON UNIT 2. **
** THERE ARE 32 ROWS AND 32 COLUMNS OF DATA. **
** EXECUTION TIME = 0 MINUTES, 16.516 SECONDS **
**
*****
```

```

**                                     **
**                                     **
*****                               *****
**                                     **
**                                     **
*****                               *****
**                                     **
** PROGRAM HAS PASSED ENTRY POINT 400.    **
**                                     **
** DATA IS CURRENTLY ON UNIT 2.          **
**                                     **
** SPARE TAPE IS CURRENTLY ON UNIT 1.      **
**                                     **
** THERE ARE 32 ROWS AND 32 COLUMNS OF DATA. **
**                                     **
** EXECUTION TIME = 1 MINUTES, 3.427 SECONDS **
**                                     **
**                                     **

```

```
*****
**
** PROGRAM HAS PASSED ENTRY POINT 500.
**
** DATA IS CURRENTLY ON UNIT 1.
**
** SPARE TAPE IS CURRENTLY ON UNIT 2.
**
** THERE ARE 32 ROWS AND 32 COLUMNS OF DATA.
**
** EXECUTION TIME = 0 MINUTES, 9.347 SECONDS
**
*****
```

\*\*\*\*\*  
\*\* PROGRAM HAS PASSED ENTRY POINT 600. \*\*  
\*\* DATA IS CURRENTLY ON UNIT 2. \*\*  
\*\* SPARE TAPE IS CURRENTLY ON UNIT 1. \*\*  
\*\* THERE ARE 32 ROWS AND 32 COLUMNS OF DATA. \*\*  
\*\* EXECUTION TIME = 1 MINUTES, 1.521 SECONDS \*\*  
\*\*\*\*\*

\*\*\*\*\*  
\*\* PROGRAM HAS PASSED ENTRY POINT 700. \*\*  
\*\* DATA IS CURRENTLY ON UNIT 1. \*\*  
\*\* SPARE TAPE IS CURRENTLY ON UNIT 2. \*\*  
\*\* THERE ARE 32 ROWS AND 32 COLUMNS OF DATA. \*\*  
\*\* EXECUTION TIME = 0 MINUTES, 26.222 SECONDS \*\*  
\*\*\*\*\*

\*\*\*\*\*  
\*\* PROGRAM HAS PASSED ENTRY POINT 800. \*\*  
\*\* DATA IS CURRENTLY ON UNIT 2. \*\*  
\*\* SPARE TAPE IS CURRENTLY ON UNIT 1. \*\*  
\*\* THERE ARE 32 ROWS AND 32 COLUMNS OF DATA. \*\*  
\*\* EXECUTION TIME = 1 MINUTES, 8.054 SECONDS \*\*  
\*\*\*\*\*

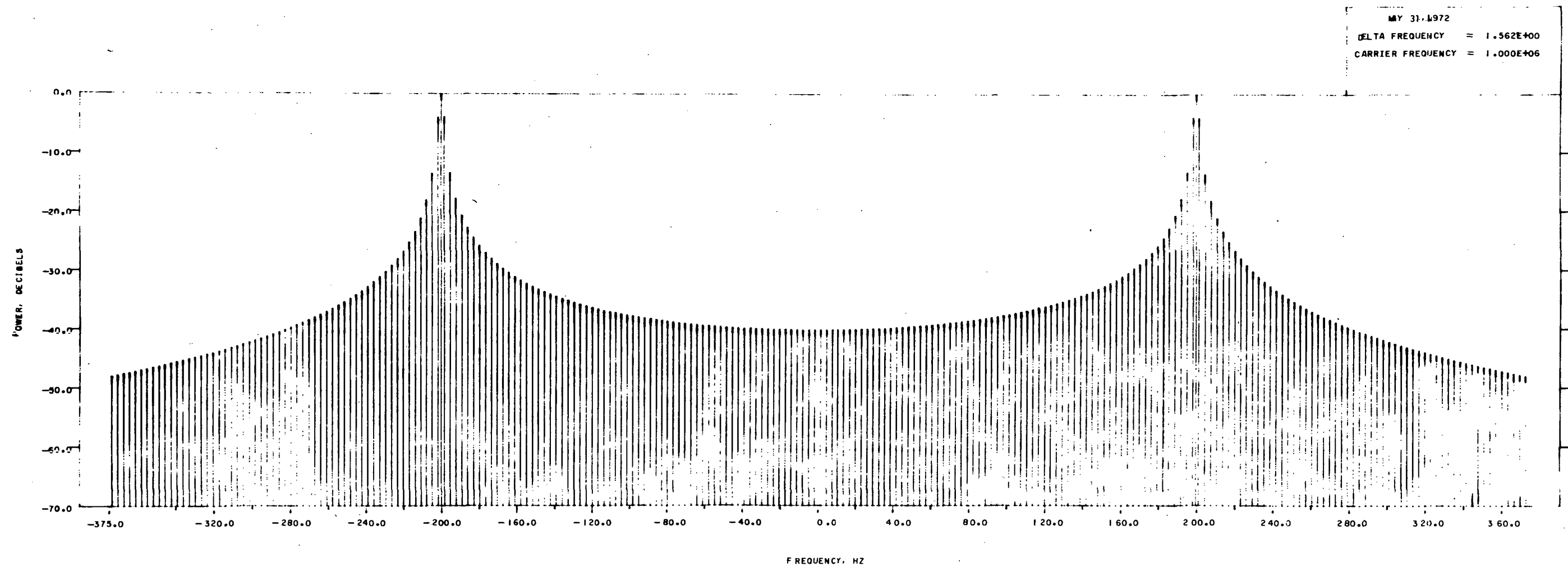
\*\*\*\*\*  
\*\* PROGRAM HAS PASSED ENTRY POINT 900. \*\*  
\*\* DATA IS CURRENTLY ON UNIT 2. \*\*  
\*\* SPARE TAPE IS CURRENTLY ON UNIT 1. \*\*  
\*\* THERE ARE 32 ROWS AND 32 COLUMNS OF DATA. \*\*  
\*\* EXECUTION TIME = 0 MINUTES, 0.816 SECONDS \*\*  
\*\*\*\*\*

\*\*\*\*\*  
\*\* PROGRAM HAS PASSED ENTRY POINT 1000. \*\*  
\*\* DATA IS CURRENTLY ON UNIT 1. \*\*  
\*\* SPARE TAPE IS CURRENTLY ON UNIT 2. \*\*  
\*\* THERE ARE 32 ROWS AND 32 COLUMNS OF DATA. \*\*  
\*\* EXECUTION TIME = 0 MINUTES, 6.806 SECONDS \*\*  
\*\*\*\*\*



0.9997200100	-0.39414563E02	0.99990781E06	-0.38175606E02	0.10000953E07	-0.38008700E02	0.10002828E07	-0.39794136E02
0.99972137E06	-0.70000000E02	0.99990937E06	-0.70000000E02	0.10000969E07	-0.70000000E02	0.10002884E07	-0.70000000E02
0.99972263E06	-0.35020960E02	0.99991094E06	-0.37333406E02	0.10000984E07	-0.37833188E02	0.10002895E07	-0.40160958E02
0.99972390E06	-0.70000000E02	0.99991250E06	-0.70000000E02	0.10001000E07	-0.70000000E02	0.10002906E07	-0.70000000E02
0.99972517E06	-0.36812457E02	0.99991406E06	-0.38484557E02	0.10001015E07	-0.37674760E02	0.10002917E07	-0.40515344E02
0.99972644E06	-0.70000000E02	0.99991562E06	-0.70000000E02	0.10001031E07	-0.70000000E02	0.10002928E07	-0.70000000E02
0.99972771E06	-0.38100000E02	0.99991719E06	-0.38627293E02	0.10001047E07	-0.37452971E02	0.10002939E07	-0.40859212E02
0.99972898E06	-0.70000000E02	0.99991875E06	-0.70000000E02	0.10001062E07	-0.70000000E02	0.10002950E07	-0.70000000E02
0.99973025E06	-0.37745078E02	0.99992031E06	-0.38762703E02	0.10001078E07	-0.37247717E02	0.10002961E07	-0.41192308E02
0.99973152E06	-0.70000000E02	0.99992187E06	-0.70000000E02	0.10001094E07	-0.70000000E02	0.10002972E07	-0.70000000E02
0.99973279E06	-0.37283922E02	0.99992344E06	-0.38890981E02	0.10001109E07	-0.37031491E02	0.10002983E07	-0.41516294E02
0.99973406E06	-0.70000000E02	0.99992500E06	-0.70000000E02	0.10001125E07	-0.70000000E02	0.10003000E07	-0.70000000E02
0.99973533E06	-0.38801144E02	0.99992656E06	-0.39012591E02	0.10001141E07	-0.36803463E02	0.10003016E07	-0.41828780E02
0.99973660E06	-0.70000000E02	0.99992813E06	-0.70000000E02	0.10001156E07	-0.70000000E02	0.10003031E07	-0.70000000E02
0.99973787E06	-0.38294762E02	0.99992969E06	-0.39127507E02	0.10001172E07	-0.36563058E02	0.10003047E07	-0.42134844E02
0.99973914E06	-0.70000000E02	0.99993125E06	-0.70000000E02	0.10001187E07	-0.70000000E02	0.10003062E07	-0.70000000E02
0.99974041E06	-0.35762255E02	0.99993281E06	-0.39236144E02	0.10001203E07	-0.36309248E02	0.10003078E07	-0.42431984E02
0.99974168E06	-0.70000000E02	0.99993437E06	-0.70000000E02	0.10001219E07	-0.70000000E02	0.10003094E07	-0.70000000E02
0.99974295E06	-0.35201074E02	0.99993594E06	-0.39338625E02	0.10001234E07	-0.36041214E02	0.10003109E07	-0.42721480E02
0.99974422E06	-0.70000000E02	0.99993750E06	-0.70000000E02	0.10001250E07	-0.70000000E02	0.10003125E07	-0.70000000E02
0.99974549E06	-0.34608031E02	0.99993906E06	-0.39435225E02	0.10001266E07	-0.35757530E02	0.10003141E07	-0.43003343E02
0.99974676E06	-0.70000000E02	0.99994062E06	-0.70000000E02	0.10001281E07	-0.70000000E02	0.10003156E07	-0.70000000E02
0.99974803E06	-0.33977264E02	0.99994219E06	-0.39526011E02	0.10001297E07	-0.35457415E02	0.10003172E07	-0.43278501E02
0.99974930E06	-0.70000000E02	0.99994375E06	-0.70000000E02	0.10001312E07	-0.70000000E02	0.10003187E07	-0.70000000E02
0.99975057E06	-0.33304901E02	0.99994531E06	-0.39611223E02	0.10001328E07	-0.35139125E02	0.10003203E07	-0.43566880E02
0.99975184E06	-0.70000000E02	0.99994687E06	-0.70000000E02	0.10001343E07	-0.70000000E02	0.10003219E07	-0.70000000E02
0.99975311E06	-0.32584071E02	0.99994844E06	-0.39690916E02	0.10001359E07	-0.34800197E02	0.10003234E07	-0.43809192E02
0.99975438E06	-0.70000000E02	0.99995000E06	-0.70000000E02	0.10001375E07	-0.70000000E02	0.10003250E07	-0.70000000E02
0.99975565E06	-0.31807123E02	0.99995156E06	-0.39765474E02	0.10001391E07	-0.34441581E02	0.10003266E07	-0.44064893E02
0.99975692E06	-0.70000000E02	0.99995312E06	-0.70000000E02	0.10001406E07	-0.70000000E02	0.10003281E07	-0.70000000E02
0.99975819E06	-0.30963480E02	0.99995469E06	-0.39834654E02	0.10001422E07	-0.34058354E02	0.10003297E07	-0.44315454E02
0.99975946E06	-0.70000000E02	0.99995625E06	-0.70000000E02	0.10001437E07	-0.70000000E02	0.10003312E07	-0.70000000E02
0.99976073E06	-0.30042335E02	0.99995781E06	-0.39888813E02	0.10001453E07	-0.33648802E02	0.10003328E07	-0.44560283E02
0.99976200E06	-0.70000000E02	0.99995937E06	-0.70000000E02	0.10001469E07	-0.70000000E02	0.10003343E07	-0.70000000E02
0.99976327E06	-0.29019464E02	0.99996094E06	-0.39957974E02	0.10001484E07	-0.33210202E02	0.10003359E07	-0.44808025E02
0.99976454E06	-0.70000000E02	0.99996250E06	-0.70000000E02	0.10001500E07	-0.70000000E02	0.10003375E07	-0.70000000E02
0.99976581E06	-0.27877464E02	0.99996406E06	-0.40012281E02	0.10001516E07	-0.32738251E02	0.10003391E07	-0.45034448E02
0.99976708E06	-0.70000000E02	0.99996562E06	-0.70000000E02	0.10001531E07	-0.70000000E02	0.10003406E07	-0.70000000E02
0.99976835E06	-0.26578622E02	0.99996719E06	-0.40061753E02	0.10001547E07	-0.32229830E02	0.10003422E07	-0.45264351E02
0.99976962E06	-0.70000000E02	0.99996875E06	-0.70000000E02	0.10001562E07	-0.70000000E02	0.10003437E07	-0.70000000E02
0.99977089E06	-0.25071382E02	0.99997031E06	-0.40106513E02	0.10001578E07	-0.31679006E02	0.10003453E07	-0.45489482E02
0.99977216E06	-0.70000000E02	0.99997187E06	-0.70000000E02	0.10001594E07	-0.70000000E02	0.10003469E07	-0.70000000E02
0.99977343E06	-0.24271413E02	0.99997344E06	-0.40146592E02	0.10001609E07	-0.31079678E02	0.10003484E07	-0.45710622E02
0.99977470E06	-0.70000000E02	0.99997500E06	-0.70000000E02	0.10001625E07	-0.70000000E02	0.10003500E07	-0.70000000E02
0.99977597E06	-0.21031134E02	0.99997656E06	-0.40182115E02	0.10001641E07	-0.30423667E02	0.10003516E07	-0.45928174E02
0.99977724E06	-0.70000000E02	0.99997812E06	-0.70000000E02	0.10001656E07	-0.70000000E02	0.10003531E07	-0.70000000E02
0.99977851E06	-0.18050402E02	0.99997968E06	-0.40213046E02	0.10001672E07	-0.29701113E02	0.10003547E07	-0.46138927E02
0.99977978E06	-0.70000000E02	0.99998125E06	-0.70000000E02	0.10001687E07	-0.70000000E02	0.10003562E07	-0.70000000E02
0.99978105E06	-0.13554741E02	0.99998281E06	-0.40239491E02	0.10001703E07	-0.28898589E02	0.10003578E07	-0.46347262E02
0.99978232E06	-0.70000000E02	0.99998437E06	-0.70000000E02	0.10001719E07	-0.70000000E02	0.10003594E07	-0.70000000E02
0.99978359E06	-0.39529604E01	0.99998594E06	-0.40262446E02	0.10001734E07	-0.27998680E02	0.10003609E07	-0.46559335E02
0.99978486E06	-0.14263706E-06	0.99998750E06	-0.70000000E02	0.10001750E07	-0.70000000E02	0.10003625E07	-0.70000000E02
0.99978613E06	-0.36930186E01	0.99998906E06	-0.40279015E02	0.10001766E07	-0.26976662E02	0.10003641E07	-0.46752597E02
0.99978740E06	-0.70000000E02	0.99999062E06	-0.70000000E02	0.10001781E07	-0.70000000E02	0.10003656E07	-0.70000000E02
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0.99978994E06	-0.70000000E02	0.99999375E06	-0.70000000E02	0.10001813E07	-0.70000000E02	0.10003687E07	-0.70000000E02
0.99979121E06	-0.17750807E02	0.99999531E06	-0.40308897E02	0.10001828E07	-0.24411345E02	0.10003703E07	-0.47143815E02
0.99979248E06	-0.70000000E02	0.99999687E06	-0.70000000E02	0.10001844E07	-0.70000000E02	0.10003719E07	-0.70000000E02
0.99979375E06	-0.20511215E02	0.99999844E06	-0.40303273E02	0.10001859E07	-0.22731643E02	0.10003734E07	-0.47334567E02
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0.99980000E06	*****	0.99999999E06	*****	0.10002154E07	*****	0.10004029E07	*****
0.99980000E06	*****	0.99999999E06	*****	0.10002169E07	*****	0.10004044E07	*****
0.99980000E06	*****	0.99999999E06	*****	0.10002185E07	*****	0.10004060E07	*****
0.99980000E06	*****	0.99999999E06	*****	0.10002199E07	*****	0.10004075E07	*****
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0.99980000E06	*****	0.99999999E06	*****	0.10002261E07	*****	0.10004137E07	*****
0.99980000E06	*****	0.99999999E06	*****	0.10002277E07	*****	0.10004153E07	*****
0.99980000E06	*****	0.99999999E06	*****	0.10002292E07	*****	0.10004168E07	*****
0.99980000E06	*****	0.99999999E06	*****	0.10002308E07	*****	0.10004184E07	*****
0.99980000E06	*****	0.99999999E06	*****	0.10002323E07	*****	0.10004199E07	*****
0.99980000E06	*****	0.99999999E06	*****	0.10002339E07	*****	0.10004215E07	*****
0.99980000E06	*****	0.99999999E06	*****	0.10002354E07	*****	0.10004230E07	*****
0.99980000E06	*****	0.99999999E06	*****	0.10002370E07	*****	0.10004246E07	*****
0.99980000E06	*****	0.99999999E06	*****	0.10002385E07	*****	0.10004261E07	*****
0.99980000E06	*****	0.99999999E06	*****	0.10002401E07	*****	0.10004277E07	*****
0.99980000E06	*****	0					





The theoretical results for this example are given by Reference 12

$$P(n\Delta f) = 20 \log \left\{ \frac{2\beta \sin[(\beta-n) \pi/2]}{\pi(\beta^2 - n^2)} \right\} - 20 \log P_{\text{ref}}$$

$P(n\Delta f)$  is the power (in decibels) in the  $n$  spectral component,  $P_{\text{ref}}$  is selected to be the maximum power component, and  $\beta$  is the peak frequency deviation.



## 2.3 MEASUREMENT AND INTERFACE HARDWARE DESIGN

This section discusses the design of a data acquisition system for the UNIVAC 1230 computer which will acquire, digitize, and record on magnetic tape a wideband input modulating signal for the spectral analysis program. The system described provides a general utility design which also permits acquisition of wideband analog signals not specifically related to the spectral analysis program. In principle, the data acquisition system accepts a wideband analog signal, performs periodic sampling of the input signal, performs an analog-to-digital (A/D) conversion of each input sample, and supplies the resultant digital signals to the UNIVAC 1230 computer at a rate and in a form compatible with the computer functional and electrical design characteristics.

### 2.3.1 Computer Interface Requirements

The UNIVAC 1230 computer Technical Description and Input/Output Design Characteristics literature states that the computer's "slow interface" provides input/output (I/O) communications transfer rates up to a maximum of 41,666 30-bit words/sec. for one channel, or up to a maximum of 333,333 30-bit words/sec. for multichannel operation. The "fast interface" of the computer provides up to 166,667 30-bit words/sec. on one channel, or up to 500,000 30-bit words/sec. on three or more channels.

The access to each I/O communications channel is through two cables. The input cable contains 30 data-bit lines plus four control signal lines; the output cable contains 30 data-bit lines plus four control signal lines, as shown in Figure 2-13. The control signals and their definitions are described in Table 2-4.

In the interest of minimizing the complexity of the external computer interface hardware, only the input cable will be used, since the data acquisition system will only be inputting data to the computer. The system employs an external interrupt to cause the computer to initialize its input buffer and uses the computer's acknowledgement of this interrupt as a signal to begin inputting data words to the computer.

Table 2-4. Control Signals Used in Input/Output

Channel	Signal Name	Origin	Meaning
Input	Interrupt Enable (IE)	Computer	"I have enabled my input section to honor an Interrupt on your channel."
	Input Data Request (IDR)	Peripheral Equipment	"I have a data word on my output lines ready for you to accept."
	Input Acknowledge (IA)	Computer	"I have sampled your data lines."
	External Interrupt (INT)	Peripheral Equipment	"I have an Interrupt code word on my output lines ready for you to accept."
Output	Output Data Request (ODR)	Peripheral Equipment	"I am in a condition to accept a word of data from you."
	Output Acknowledge (OA)	Computer	"I have put a data word for you on the data lines; sample them now."
	External Function Request (EFR)	Peripheral Equipment	"I am in a condition to accept an External Function message on my data lines."
	External Function (EF)	Computer	"I have put an External Function message for you on the data lines; sample them now."

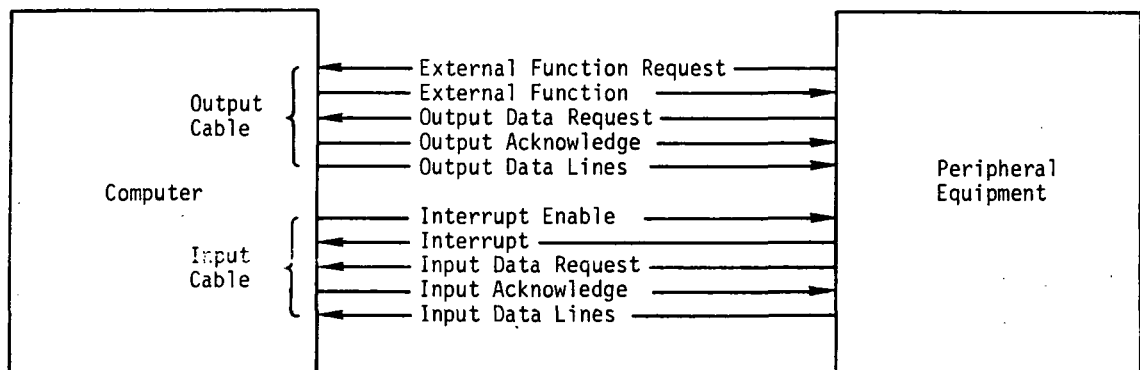


Figure 2-13. Computer-to-Peripheral Equipment Interface

The (simplified) sequence of events for the interrupt dialog is as follows:

1. The computer sets the Interrupt Enable when it is ready to accept an External Interrupt.
2. The peripheral equipment (the external computer interface hardware) detects the Interrupt Enable.
3. If the peripheral equipment status requires the computer to be interrupted (system ready to begin acquiring input data samples), it sets the External Interrupt line.\*
4. The computer detects the setting of the External Interrupt line.
5. In accordance with internal priorities, the computer initiates its input buffer under software control.
6. The computer clears the Interrupt Enable line and sets the Input Acknowledge line.\*\*
7. The peripheral equipment detects the simultaneous setting of the Input Acknowledge line and the clearing of the Interrupt Enable line.
8. The peripheral equipment may clear the External Interrupt line at any time after detecting this simultaneous occurrence of conditions, but it must clear the External Interrupt line before the computer will recognize the next interrupt.
9. The computer clears the Input Acknowledge line before it reads the future contents of the Input Data Lines.

---

\* No External Interrupt Code word is required for operation of the data acquisition system.

\*\* The simultaneous occurrence of these conditions is used by the peripheral equipment to differentiate between the "acknowledge" of an interrupt and that of an input data request.

The normal input sequence for data transfer from the peripheral equipment to the computer is as follows:

1. The computer initiates an input buffer for the given input channel (as in step 5 above).
2. The peripheral equipment places a word of data on the Input Data lines.
3. The peripheral equipment sets the Input Data Request line to indicate that a word of data is on the Input Data lines.
4. The computer senses the setting of the Input Data Request line.
5. In accordance with internal priorities, the computer reads the data word currently present on the Input Data lines.
6. The computer sets the Input Acknowledge line to indicate that it has read the data word on the Input Data lines.
7. The peripheral equipment detects the setting of the Input Acknowledge line.
8. The peripheral equipment may clear the Input Data Request line at any time after detecting the setting of the Input Acknowledge line, but it must clear the Input Data Request before the computer will recognize the next Input Data Request.
9. The computer clears the Input Acknowledge line before it reads the next word on the Input Data lines.

Steps 2 through 9 of this sequence are repeated for every data word until the number of words specified in the input buffer have been transferred to the computer.

The following requirements apply to the timing of control signals and data lines between the computer and peripheral equipment.

1. Data lines must be stable at the time they are gated into storage elements. They need not be cleared to the "zero" state between successive words, as is the case with control lines. For input, the computer provides a delay between the detection of the Input Data Request and the sampling of the Input Data lines.

2. An External Interrupt or Input Data Request signal, once set, must remain in that state until it is acknowledged. Otherwise, there is a risk of destroyed or lost data, or an unexecuted command.
3. All control lines must return to the logical "zero" state between successive application and recognition of control signals. Synchronization of events is accomplished by sensing a control signal's transition from the "zero" to the "one" state.
4. Any input circuit, receiving data or control information from an intercommunication cable, will treat an open circuit or disconnected input wire as though a "zero" were present at the input.

When the computer sets the Input Acknowledge signal in response to an interrupt, it clears the Interrupt Enable and will not reset it again until enabled by the computer program. To ensure that an interrupt will be accepted, the External Interrupt signal should be maintained on the line until the Interrupt Enable is dropped and the Input Acknowledge is set (a simultaneous occurrence). The minimum delay between sensing the External Interrupt and acknowledging is  $2.4 \mu\text{sec}$ ; there is no maximum limit for this delay, since for a particular cycle, the delay is determined by the interaction with the computer program and the other input/output channels. In this case, the delay primarily will be that required to initiate the input buffer.

To ensure that input data is accepted, the Input Data Request and the data must be maintained on the lines until an answering Input Acknowledge is received. The Input Data Request may be activated at the same time, or it may set after, the data lines are set. The minimum time delay between sensing the Input Data Request and the answering Input Acknowledge is  $2.4 \mu\text{sec}$ . As with the interrupt, there is no maximum time limit on this delay.

The Input Acknowledge is set for a fixed time interval, whether the Input Data Request is dropped right away or not; the minimum Input Acknowledge duration is  $2.2 \mu\text{sec}$ . At least  $1.2 \mu\text{sec}$ . must expire between dropping the Input Data Request and reactivating it.

### 2.3.2 Hardware Design Trade-off

The primary trade-off in the design of the data acquisition hardware is the method to be used for buffering or storing the input data prior to loading it into the computer. If the input sampling rates were always to be 100 kHz or less, the EMI Analog Multiplexer-Quantizer (AMQ) could be used. But the required data acquisition system must be capable of handling wideband analog signals up to 4.5 MHz-wide color TV video (which requires input sampling rates of at least on the order of 10 MHz).

The candidate storage techniques are:

1. High-speed serial shift registers,
2. Wideband video tape,
3. High speed disc, and
4. Core memory.

All items require an analog-to-digital (A/D) converter to convert the analog input signal into digital form. Items 1, 3, and 4 convert prior to storage, while item 2 converts upon readout from storage.

Taking the candidates in reverse order, core memory can provide the required resolution (and hence a desirable, inherently high quantizing signal-to-noise ratio, or SNR), but it is too slow and is quite expensive. High-speed disc, while retaining a desirable high SNR, is even slower than core memory and is still fairly expensive. Video tape is relatively inexpensive but has three significant disadvantages: 1) an inherently low SNR ( $\sim 30$  dB), 2) unavoidable flutter, wow, and time jitter, and 3) poor low-frequency response (cutoff at  $\sim 400$  Hz). If the nominal input rate to the computer were 100 kHz, input data that would otherwise require a 10 MHz sampling rate would have to be recorded and then played back at 1/100-th of the recording speed. Even if tape speed fluctuations during recording were unimportant, the effective low-frequency cutoff of the record/playback process would be  $\sim 40$  kHz.

The high-speed serial shift register thus emerges as the only candidate which can operate with the required speed and provide the necessary SNR, wideband response, and precision timing. The shift register can be loaded from an A/D converter capable of sampling up to  $\sim 10$  MHz, and then, after all input samples are loaded, the register can be clocked-out at  $\sim 100$  kHz into the computer.

Even though a high-speed shift register has been selected on the basis of operating considerations, its low cost makes it even more attractive. When circuits for controlling the start, stop, and playback of the tape system are considered in addition to the tape drive, the shift-register and associated control circuitry are clearly the least expensive solution.

While an A/D converter plus shift-register scheme can be readout directly into the computer, some control circuitry is required for interfacing with the computer. As an interim measure, the EMI AMQ could be used as the interface by adding a digital-to-analog (D/A) converter at the output of the shift register. Operating at the required input sampling rate, the front-end A/D converter could load the shift-register at high speed. Then, possibly operating in a recirculation mode, where the register contents are reinserted at the input during readout, the register can be readout at a suitably-reduced rate through the output D/A converter directly into the analog input of the AMQ. The AMQ would operate as if the original signal had been "narrow-band", and the computer would be loaded with suitable digital data samples. Such operation is analogous to that envisioned with a reduced playback-speed video tape system, except that SNR, time errors, and low-frequency cutoff are not problems.

### 2.3.3 Data Acquisition System Block Diagram

As an option, the spectral analysis program will operate on data input from a digital magnetic tape. The data acquisition system outlined in Figure 2-14 converts an arbitrary input signal  $\phi(t)$  into the required formatted digital samples and records them on magnetic tape for subsequent input to the spectral analysis program. Figure 2-14 is a first-level block diagram showing the data acquisition system organized into seven operational units:

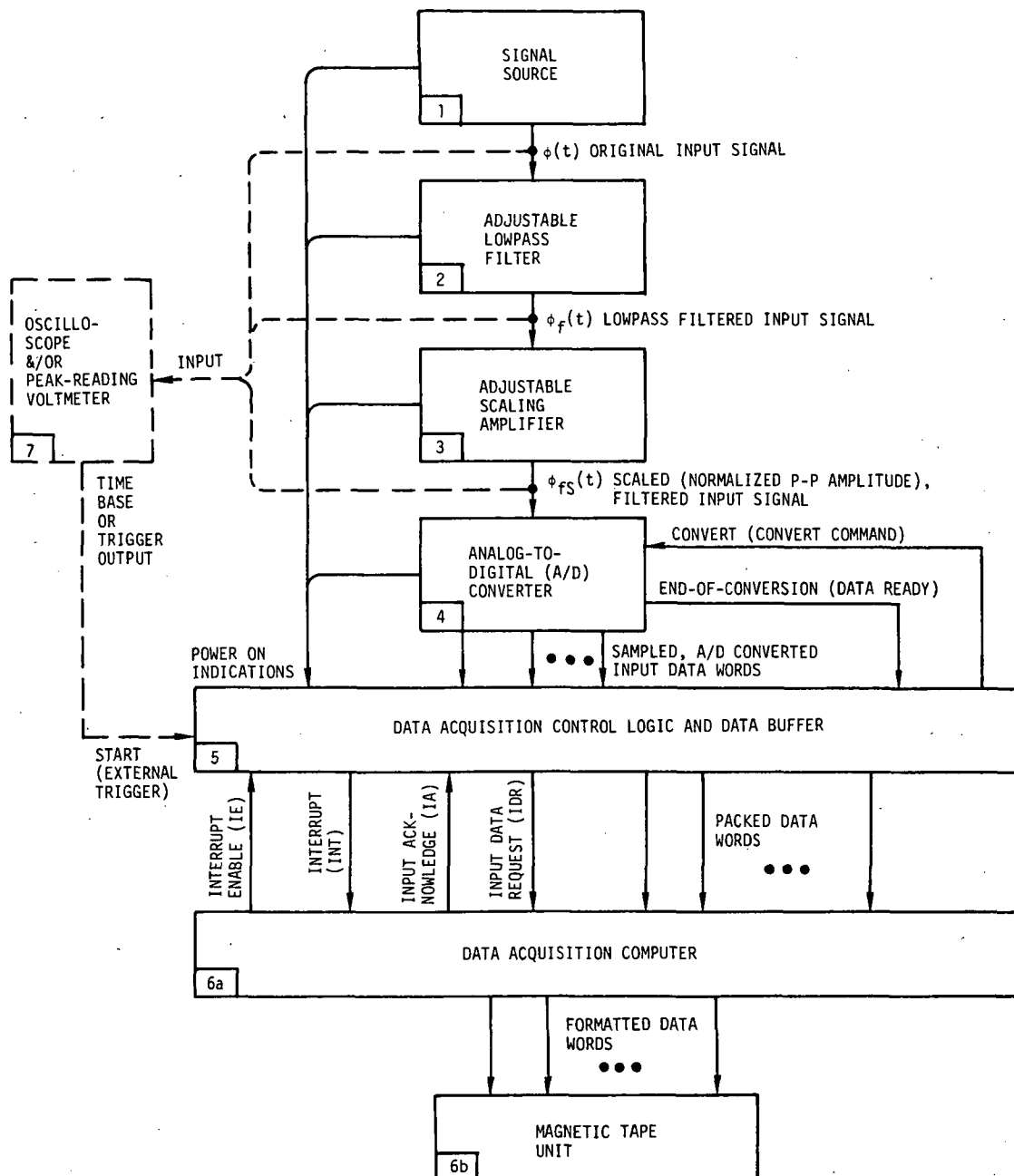


Figure 2-14. Data Acquisition System



- Unit 1. Signal Source,
- Unit 2. Adjustable Lowpass Filter,
- Unit 3. Adjustable Scaling Amplifier,
- Unit 4. Analog-to-digital (A/D) Converter,
- Unit 5. Data Acquisition Control Logic and Data Buffer,
- Unit 6. Data Acquisition Computer (including the Magnetic Tape Unit), and
- Unit 7. (Optional) Oscilloscope and/or Peak-Reading Voltmeter.

The Unit numbers facilitate assignment of reference designations for the various elements of the data acquisition system.

The signal source (Unit 1) generates or supplies the input analog signal  $\phi(t)$ , which is to be processed by the data acquisition system for subsequent input to the spectral analysis program. The lowpass filter (Unit 2) bandlimits this signal to assure that aliasing does not occur in the sampling process; the filter cutoff frequency is adjusted so that the maximum frequency ( $f_{\max}$ ) in the resultant filtered signal  $\phi_f(t)$  is less than half of the input sampling rate. To assure that the full input dynamic range of the converter is used, the gain of the scaling amplifier (Unit 3) is adjusted to normalize the peak-to-peak amplitude of the filtered signal, presenting a standard-level signal  $\phi_{fs}(t)$  to the converter.

Under the control of carefully-timed sampling pulses (the "CONVERT", or "CONVERT COMMAND", signal), the A/D converter (Unit 4) samples  $\phi_{fs}(t)$  during a very short time interval or sampling window, holds this sampled value during the conversion process (sample-and-hold), and converts or encodes this analog value to an equivalent binary number or digital word. When the conversion of each input sample is complete, and the corresponding digital word is available at the converter output, the converter generates an "END-OF-CONVERSION", or "DATA READY", pulse.

The data acquisition control logic and data buffer (Unit 5) controls the timing of the input sampling process, provides buffer storage for the acquired data samples, assembles data words for transmission to the computer,

and handles the event sequencing and detailed dialog with the computer. By means of a suitable software program, the data acquisition computer (Unit 6) interacts with the data acquisition control logic and data buffer, converts the acquired data samples into the format required by the spectral analysis program, and writes the formatted data samples on magnetic tape. The resultant tape(s) can be used with the tape input option of the spectral analysis program.

The (optional) oscilloscope and/or peak-reading voltmeter (Unit 7) can be used to monitor the  $\phi(t)$ ,  $\phi_f(t)$ , and/or  $\phi_{fs}(t)$  signals. This monitoring function, or equivalent, is required when setting the gain of the scaling amplifier. When a repetitive signal is to be sampled, the scope can be triggered at some point on the waveform, and the resultant scope time base or trigger output signal can be used to automatically initiate a data acquisition sequence.

#### 2.3.4 Basic Operational Description

To operate the data acquisition system, the operator turns on the signal source, lowpass filter, scaling amplifier, A/D converter, data acquisition control logic and data buffer, data acquisition computer, magnetic tape unit, and oscilloscope and/or voltmeter. While the units are warming up, he then sets the cutoff frequency of the lowpass filter and selects an appropriate sample rate (controlled by the data acquisition control logic, Unit 5). Once the signal source, lowpass filter, scaling amplifier, and oscilloscope and/or voltmeter have stabilized, the operator adjusts the gain of the scaling amplifier until the peak-to-peak amplitude of  $\phi_{fs}(t)$  is equal to the full-scale rating of the A/D converter.

Also on Unit 5, he selects whether the data acquisition sequence is to be started manually (via a "START" pushbutton on Unit 5) or automatically (via the scope trigger output, or some other suitable triggering source), and whether at the conclusion of the data acquisition sequence the system is to be reset manually (via a "RESET" pushbutton on Unit 5) or automatically (via the appropriate dialog exchange with the computer). If automatic

starting is selected, the operator then sets the scope time base triggering to start sweeping at the desired point on the  $\phi(t)$ ,  $\phi_f(t)$ , or  $\phi_{fs}(t)$  waveform.

After setting up the acquisition hardware (Units 1 through 5, and 7), the operator mounts a magnetic tape on the tape drive (Unit 6b) and loads the data acquisition program into the computer (Unit 6a). Once all of the hardware has been configured, the tape mounted, and the program loaded, the data acquisition system is ready for acquiring samples of  $\phi_{fs}(t)$ .

#### 2.3.4.1 Data Acquisition Initiation Sequence

When loaded and started, the data acquisition program activates the "INTERRUPT ENABLE" (IE) signal and, if an "INTERRUPT" (INT) is not received by the time a runout or "watchdog" timer expires one or more times, prints out one or more error messages. If Units 1 through 4 are "ON" (indicated by suitable logic signals from each unit) and (IE) is active, the control logic (Unit 5) periodically activates the (INT) signal until it is acknowledged ("INPUT ACKNOWLEDGE (IA)" raised simultaneously with "(IE)" dropped).\*

When an interrupt is received, the computer initializes its input buffer and acknowledges the interrupt. Once the interrupt is acknowledged, both the hardware and computer are ready to begin processing input samples of  $\phi_{fs}(t)$ .

#### 2.3.4.2 Data Acquisition Sampling Sequence

At the completion of the initiation interrupt/acknowledge dialog, the control logic (Unit 5) is configured to begin taking samples of the input signal. If manual starting has been selected, the data acquisition system waits until the operator depresses the "START" pushbutton. If automatic starting has been selected, sampling starts as soon as a start pulse is received from the oscilloscope or other source.

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\* The computer operation may require that (INT) remain activated until acknowledged.

Once the sampling sequence is started, a series of precisely-timed "CONVERT" (or "CONVERT COMMAND") pulses are sent to the A/D converter (Unit 4). The precision sampling pulses are derived from a count-down chain (driven by a crystal oscillator) within Unit 5. The sampling rate is determined by the selected output tap on the count-down chain. When the conversion of a given input sample is complete, the converter responds with an "END-OF-CONVERSION" (EOC), or "DATA READY", pulse. The (EOC) pulse is used to load the A/D converter digital output word into a holding buffer (within Unit 5) for transmission to the computer.\*

The sampling/conversion process continues at a precisely-controlled rate until terminated either by a counter (within Unit 5) or by the computer.\* Once all conversions are completed, the control logic either continues, or starts, the readout of the data buffer into the computer.

#### 2.3.4.3 Data Transmission Sequence (Data Buffer to Computer)

A/D converter output words are loaded into the Unit 5 data buffer in groups of three. This packed format allows more efficient utilization of the bits in the computer input buffer, plus allowing a higher overall data transfer rate into the computer. When the Unit 5 control logic determines that a data word is ready for transmission to the computer, the "INPUT DATA REQUEST" (IDR) signal is raised. When the computer has stored the word in its input buffer, the "INPUT ACKNOWLEDGE" (IA) line is raised. The control logic then drops (IDR) and the computer drops (IA). The process is repeated for each subsequent data word.

If the computer responds with an (IA) after the next data word is placed on the data lines, the control logic sets an error flag in the data word. All subsequent data words will contain this error flag, indicating that one or more groups of three data samples may have been lost.

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\* The exact procedure involved will be considered in the functional description for the control logic and data buffer (Unit 5).

If an (IDR) is not followed by an (IA) before a runout timer in Unit 5 expires, the control logic assumes that the computer has filled its input buffer and will not accept any more input. The control logic then drops the (IDR) and reconfigures for subsequent reset and re-initialization.

#### 2.3.4.4 Data Formatting Sequence (Computer Software)

After the computer input buffer has been filled, the acquisition program terminates the dialog with the control logic and begins processing the stored data samples. If none of the data words contain error flags, each data word is unpacked\* as three integers. Each integer is then converted to the floating-point format required by the spectral analysis program and written on the magnetic tape.\*\*

If any of the data words contains an error flag, the current data acquisition cycle is aborted, and the computer prints out an appropriate error message. In this case, none of the acquired data samples are written on the magnetic tape.

#### 2.3.4.5 Termination or Re-initialization Sequence

When all formatted data samples have been written on the tape, or when the bad data abort described in the preceding paragraph occurs, the acquisition program either terminates, or returns to the initiation mode described above by activating the "INTERRUPT ENABLE" (IE) signal. If manual reset has been selected, the data acquisition system waits until the operator depresses the "RESET" pushbutton; the periodic error printouts can occur if the reset does not occur before the computer timer expires. If automatic reset has been selected, the control logic resets when the computer activates the (IE) signal.

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\* The unpacking can be performed with masking or shifting instructions.

\*\* The conversion process is simply a table look-up, with the integer value as an index or pointer to the appropriate entry in the table.

Once the control logic is reset, the system repeats the data acquisition initiation sequence described above, and the hardware and computer are re-configured to process a new set of input data samples. The above procedure can be repeated as often as required until all desired input samples have been processed and recorded on magnetic tape.

### 2.3.5 Theoretical Considerations

In specifying the characteristics of the data acquisition system, three items must be carefully compromised: the bandwidth (cutoff frequency and roll-off) of the lowpass filter, the input sampling rate, and the number of bits (and hence the number of quantization levels) provided by the A/D converter. These items will be discussed in reverse order, since in many respects a suitable converter will be more difficult to procure than the filter.

#### 2.3.5.1 A/D Converter Bit-Resolution

The number of bits required of the A/D converter is constrained first by the expected signal-to-noise ratio (SNR) of the input signal and second by the available size of the buffer storage words in the computer.\* The compromise here is to specify as few bits as possible, while assuring that enough bits are specified so that the resultant quantization errors are small compared to the input SNR.

The equivalent noise power of an A/D converter is shown in Figure 2-15. Here, the upper curve represents the equivalent noise of a quantizing error equal to a full least significant bit (LSB), since converters are usually specified in terms of  $\pm 1/2$  LSB accuracy. For example, a 4-bit converter (5 bits when the sign bit is included) divides the  $\pm$  full scale interval into  $\pm 16$  increments. The quantization error of  $\pm 1/2$  LSB is thus equivalent to  $1/16$  of the full scale range. Expressed in dB,  $1/16$  is equivalent to -24.1 dB (compared to a full scale of 1). A 10-bit converter (11 bits,

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\* The number of acquired data samples is constrained by computation time limitations and the available number of buffer storage words in the computer.

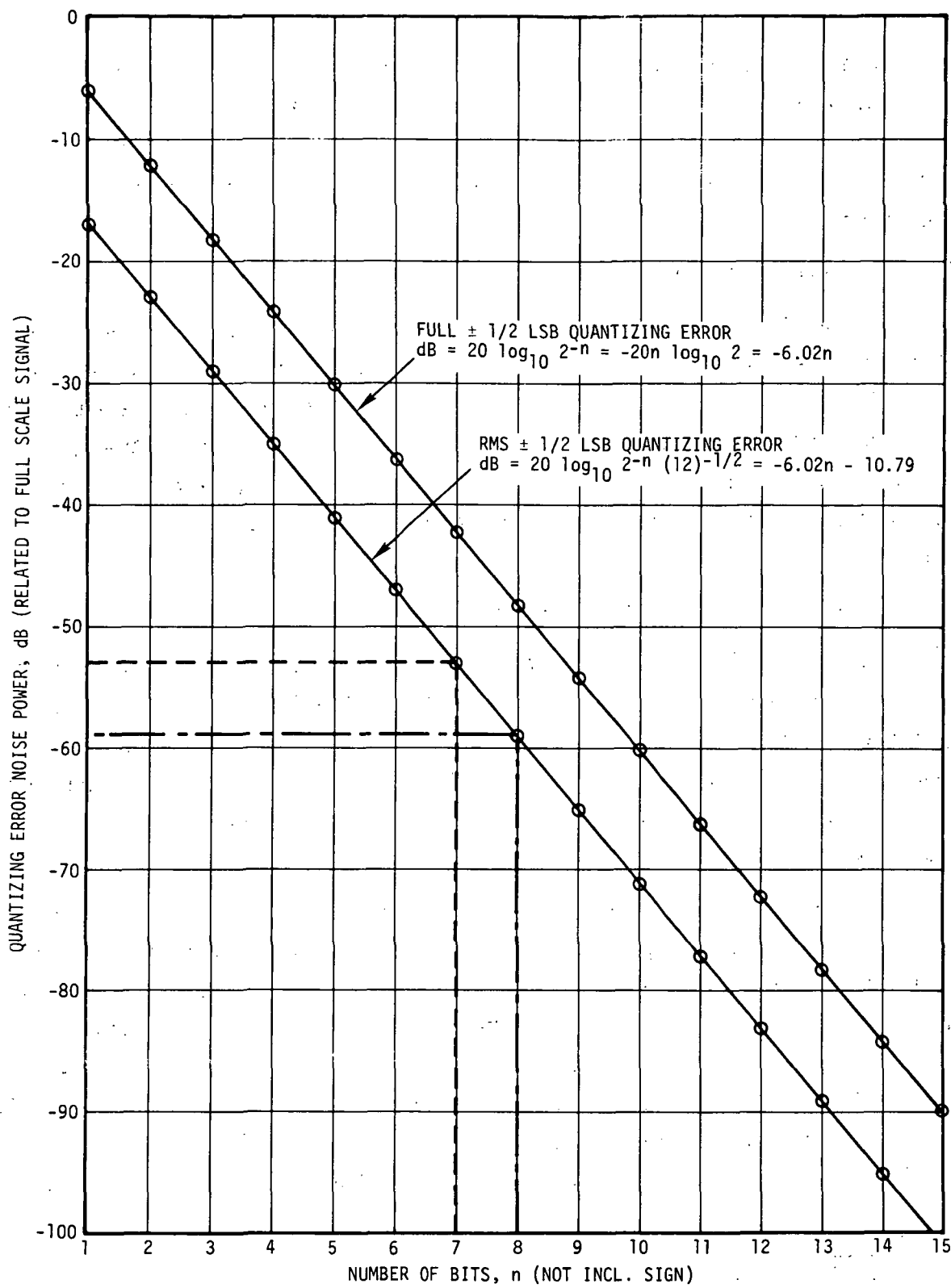


Figure 2-15. A/D Converter Quantizing Error Noise Power

including sign) divides the  $\pm$  full scale into  $\pm$  1024 increments, so  $\pm$  1/2 LSB is equivalent to 1/1024 or -60.2 dB.

If the  $\pm$  1/2 LSB quantizing error is considered to be a random variable uniformly distributed in probability over the interval  $(-1/2, +1/2)$ , the resultant rms error is  $1/\sqrt{12}$  of the full bit-error. That is, the rms error for a 4-bit converter is  $1/(\sqrt{12} \cdot 16)$  or -34.9 dB, while that for a 10-bit converter is  $1/(\sqrt{12} \cdot 1024)$  or -71.0 dB. The lower curve in Figure 2-3 is the rms quantizing error equivalent noise power.

Suppose that a 4-bit converter (5 bits, including sign) were used to process a signal having a SNR of 35 dB. After normalizing the peak-to-peak amplitude of the signal to occupy the  $\pm$  full scale dynamic range of the converter, suppose that the resultant signal power is 1.0 watt rms, which is referenced as "0 dB". The incoming rms noise power is thus -35 dB, or 0.3 mw rms. The converter introduces -35 dB rms quantization error noise power, which is also equivalent to 0.3 mw rms. Since the two rms noise powers are essentially equal, the net noise power resulting from the sum of these two is 0.6 mw rms (or 3 dB higher than either alone), for a net signal-to-noise ratio after conversion of 32 dB. If the input SNR had been 30 dB, the input rms noise power would have been 1.0 mw and the net overall rms noise power 1.3 mw, for a resultant converted SNR of 29 dB. If the input SNR had been 24 dB, the input rms noise power would have been 4.0 mw and the net overall rms noise power 4.3 mw, for a resultant converted SNR of 23.7 dB.

The purpose of this exercise has been to show that when operating with input SNR's equal to the reciprocal of the converter quantizing error, there will be a 3 dB loss in the net converted SNR (e.g., an input SNR of 35 dB will be degraded in the -35 dB, 4-bit plus sign A/D converter to a net converted SNR of 32 dB). On the other hand, operating with input SNR's that are on the order of 10 dB less or lower (input noise power > 10 times the quantization noise power), the quantization loss will be almost negligible (e.g., an input SNR of 24 dB will be degraded in the same converter to only 23.7 dB).



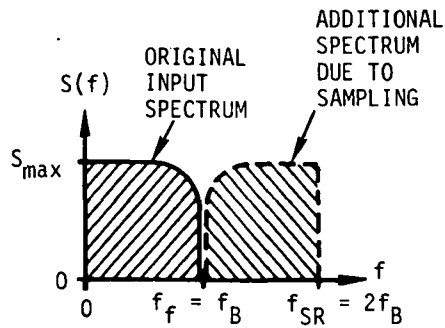
Referring to Figure 2-15, input signals having SNR's of 40 dB or less can be adequately processed by a 7-bit plus sign (8 bits total) A/D converter (-52.9 dB rms quantizing error), while an 8-bit plus sign (9 bits total) converter (-59.0 dB rms quantizing error) is suitable for input signals having SNR's of 46 dB or less. This input SNR threshold increases 6 dB as each new bit is added to the requirement.

On the basis of the above considerations, the A/D converter for the data acquisition system is chosen to be 8 bits plus sign (9 bits total), which will process input SNR's up to 46 dB with negligible quantizing error. The use of more bits would not improve the accuracy of the resultant data samples and would only unnecessarily complicate the remaining hardware processing requirements. Since the computer word is 30 bits wide, each packed data word to the computer can contain 3 data samples (27 bits), plus 3 error flag bits.

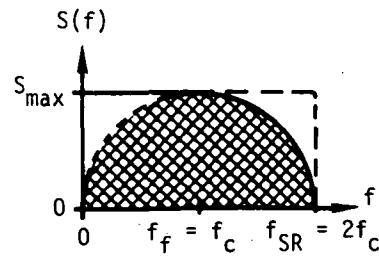
#### 2.3.5.2 A/D Converter Sample Rates

In a sampled data system, the sampling rate  $f_{SR}$  must be at least twice the bandwidth  $f_B$  of the incoming signal. For a sampling-rate-to-bandwidth ratio  $f_{SR}/f_B = 2$ , the input (lowpass) spectrum must be ideal, as in Figure 2-16a, with infinite attenuation at the cutoff frequency  $f_c = f_B = 0.5 f_{SR}$ . Note in Figure 2-16a that the original lowpass input spectrum occupies the range between  $0 \leq f \leq f_B$ . The sampling causes an identical but reversed spectrum to exist between  $f_B \leq f \leq f_{SR} = 2 f_B$ . The A/D converter operates on the input signal as if the actual input spectrum were the combination of these two spectra. Since the two spectra do not overlap, the desired sampling takes place without aliasing.

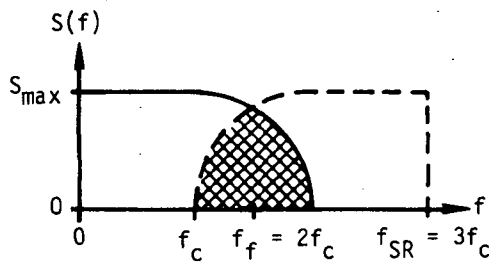
In practice, the original input spectrum will not be ideal lowpass but rather will roll-off from the cutoff frequency  $f_c$  at some (set of) dB/octave rate(s). Depending on the slope(s) of this rolloff, some degree of aliasing can be expected if the sampling rate  $f_{SR}$  is not high enough compared to the



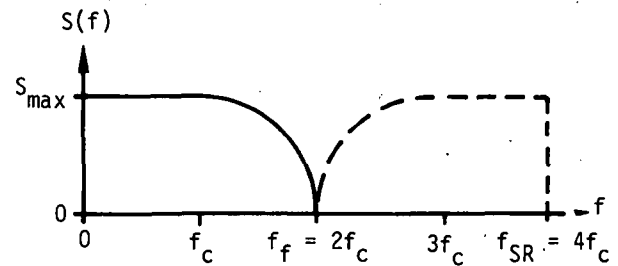
a) Ideal Lowpass Case,  
 $f_{SR} = 2f_B$  w/o Aliasing



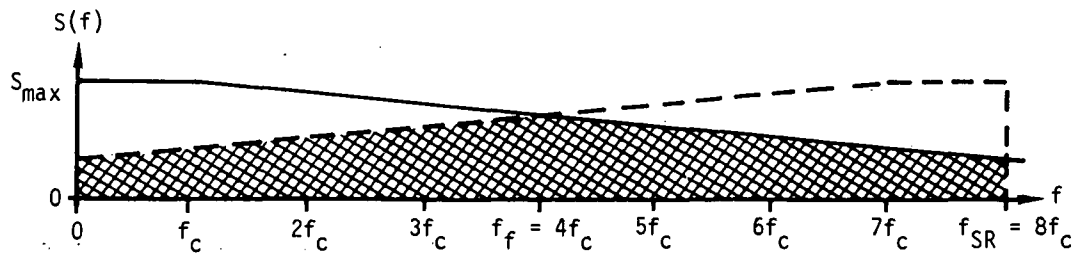
b) Undersampled Case,  
 $f_{SR} = 2f_c$  w/Considerable Aliasing



c) Undersampled Case,  
 $f_{SR} = 3f_c$  w/Some Aliasing



d) Properly-Sampled Case,  
 $f_{SR} = 4f_c$  w/Negligible Aliasing



e) Undersampled Case,  $f_{SR} = 8f_c$  w/Considerable Aliasing

Figure 2-16. Sampled Data Power Spectra

cutoff frequency  $f_c$ . Figure 2-16b shows a case where the original input spectrum starts rolling-off at  $f_c$ , is essentially negligible above  $2 f_c$ , and the sampling rate  $f_{SR} = 2 f_c$ . Note that the two spectra have considerable overlap and hence considerable aliasing. Aliasing is defined in terms of the folding frequency  $f_f = 0.5 f_{SR}$  (in this case  $f_f = f_c$ ), where an input frequency at  $f_f + \Delta f$  is interpreted by the A/D converter as being a frequency at  $f_f - \Delta f$ , where  $0 \leq \Delta f \leq f_f$ .

Figure 2-16b shows a case where the input signal is seriously under-sampled, with considerable aliasing as the result. Figure 2-4c shows the same original input spectrum, sampled at  $f_{SR} = 3 f_c$ , ( $f_f = 1.5 f_c$ ). In this case, some aliasing occurs for input frequencies above  $f_c$ . The resultant spectra for proper sampling is shown in Figure 2-16 ( $f_{SR} = r f_c$  and  $f_f = 2 f_c$ ). Here, negligible aliasing occurs, since the two spectra overlap only where the input power is negligible. Figure 2-16e shows a case where the original spectra rolls-off at 12 dB/octave (the input spectrum is thus down only 14 dB at  $2.222 f_c$ , 19 dB down at  $3 f_c$ , 24 dB down at  $4 f_c$ , 36 dB down at  $8 f_c$ , etc.). Even if the signal were sampled at a rate  $f_{SR} = 8 f_c$ , the input signal frequencies above  $f_f = 4 f_c$  will be aliased into signal frequencies below  $4 f_c$ , attenuated only 24 dB at  $4 f_c$ ; signal frequencies near  $8 f_c$  will be aliased to signal frequencies near zero and will be attenuated only 36 dB. Thus, there may be significant signal components outside the intended passband ( $f_c$ ), which due to inadequate sampling may cause undesirable aliasing effects.

Just how much aliasing the system can tolerate is constrained by the A/D converter's quantizing error. As the allowable maximum input SNR had to be lowered at least 10 dB from the reciprocal of the rms quantizing error noise power (for the effects of quantization to be negligible), so must the maximum aliasing crossover threshold at the folding frequency  $f_f = 0.5 f_{SR}$  be lowered at least 10 dB from the rms quantizing error noise power (so that the effects of aliasing are negligible). The selected converter (8 bits plus sign, or 9 bits total) has -60 dB rms quantizing error, so the aliasing crossover at  $f_f$  must be  $\lesssim -70$  dB.

If  $f_{SR} = 2 f_c$ , this -70 dB threshold requires an input spectrum roll-off above  $f_c$  of  $\infty$  dB/octave; 460 dB/octave for  $f_{SR}=2.222 f_c$  (10/4.5); 120 dB/octave for  $f_{SR} = 3 f_c$ ; 95 dB/octave for  $f_{SR}=3.333 f_c$  (15/4.5); 70 dB/octave for  $f_{SR} = 4 f_c$ ; or 53 dB/octave for  $f_{SR} = 5 f_c$ . A suitable compromise between maximum-length input time records ( $f_{SR}$  as low as possible) and reasonably gentle input spectral roll-off ( $f_{SR}$  as high as possible) would be to use  $f_{SR} = 4 f_c$ , with an input spectrum roll-off of 70 dB/octave above  $f_c$ , whenever possible. With 70 dB/octave fixed as the roll-off, the following aliasing thresholds at  $f_f = 0.5 f_{SR}$  can be achieved: 0 dB for  $f_{SR} = 2 f_c$ , -10.6 dB for  $f_{SR} = 2.222 f_c$ , -41 dB for  $f_{SR} = 3 f_c$ , -52 dB for  $f_{SR} = 3.333 f_c$ , -70 dB for  $f_{SR} = 4 f_c$ , of -93 dB for  $f_{SR} = 5 f_c$ .

The maximum bandwidth signal to be accommodated by the data acquisition system is  $f_B = 4.5$  MHz color TV video. If this signal is assumed to roll-off above  $f_c = 500$  kHz at not less than 20 dB/octave, the corresponding input spectrum, as shown in Table 2-5, will be down to  $\leq -20$  dB at 1 MHz,  $\leq -40$  dB at 2 MHz,  $\leq -60$  dB at 4 MHz,  $< -66$  dB at 5 MHz,  $< -78$  dB at 7.5 MHz, and  $< -83$  dB at 9 MHz. Similar data is included in Table 2-5 for cutoff frequencies of 1 MHz, 2 MHz, 3.75 MHz, and 4.5 MHz.

If the maximum sampling rate provided by the A/D converter is  $f_{SR} = 10$  MHz, as shown in Table 2-6, the corresponding folding frequency  $f_f = 5$  MHz and  $f_{SR} = 2.222 f_B$  (for  $f_B = 4.5$  MHz). With a 70 dB/octave roll-off above  $f_B = 4.5$  MHz, the aliasing threshold at  $f_f = 5$  MHz is -10.6 dB. To reach the required -70 dB threshold, an additional -60 dB must be provided by the roll-off in the original input signal spectrum; if the input signal rolls-off at 20 dB/octave, the corresponding cutoff frequency must be  $f_c = 625$  kHz, or less. Similar data is included in Table 2-6 for maximum sampling rates of 15 MHz and 18 MHz.

The current state-of-the-art in commercially available high-speed A/D converters appears to be 10 MHz maximum sample rate for an 8-bit plus sign (9-bit) converter. Thus, a 10 MHz sampling rate is chosen for  $f_B = 4.5$  MHz bandwidth color TV video which rolls-off at not less than 20 dB/octave above

Table 2-5. Spectral Levels for 20 dB/Octave Rolloff

Spectral Frequency $f$ (MHz)	Spectral Levels for 20 dB/Octave Rolloff (dB)				
	Starting at Cutoff Frequency $f_c$ (MHz)				
	0.50	1.00	2.00	3.75	4.50
1.0	-20	0	0	0	0
2.0	-40	-20	0	0	0
4.0	-60	-40	-20	-2	0
5.0	-66	-46	-26	-8	-3
7.5	-78	-58	-38	-20	-15
9.0	-83	-63	-43	-25	-20

Table 2-6. Sampling Parameters for  $f_B = 4.5$  MHz

Sampling Rate $f_{SR}$ (MHz)	Folding Frequency $f_f$ (MHz)	$f_{SR}/f_B$ for $f_B = 4.5$ MHz	Aliasing* Threshold (dB)	Additional Attenuation Required** (dB)	Maximum Allowable Cutoff Frequency*** $f_c$ (MHz)
10	5.0	2.222	-10.6	-60	0.625
15	7.5	3.333	-52.0	-70	3.75
18	9.0	4.000	-70.0	0	4.5 +

\* At  $f_f$ , with 70 dB/octave rolloff above  $f_B$

\*\* Above  $f_f$  to achieve -70 dB threshold

\*\*\* With 20 dB/octave rolloff to achieve -70 dB threshold

$f_c = 625$  kHz. If the TV video is not down to  $\leq -60$  dB at  $f_f = 5$  MHz and above, there will be some aliasing using a 10 MHz sampling rate. Starting with the 5 MHz entries from Table 2-5, and including -10 dB for the 70 dB/octave roll-off from 4.5 MHz, the expected degree of aliasing would be on the order of -56 dB for  $f_c = 1$  MHz, -36 dB for  $f_c = 2$  MHz, -18 dB for  $f_c = 3.75$  MHz, or -13 dB for  $f_c = 4.5$  MHz.

#### 2.3.5.3 Lowpass Filter Characteristics

The preceding discussion of A/D converter sampling rates has dealt with aliasing in terms of an assumed input spectral bandwidth  $f_B$  and cutoff frequency  $f_c$ , the sampling rate frequency  $f_{SR}$ , and the folding frequency  $f_f = 0.5 f_{SR}$ . Except for color TV video,  $f_{SR} = 4 f_c$  will be used, with a filter roll-off above  $f_c$  of 70 dB/octave. The same filter characteristics will be used for all sampling rates, as shown in Figure 2-17.

Figure 2-17 shows the envelope (shaded area) within which the gain of the lowpass filter transfer function must lie. If a signal having a uniform power spectrum were input to the filter, Figure 2-17 would correspond to the resultant power spectrum of the output of the filter. Note that the filter is allowed up to 0.5 dB ripple in the passband up to the cutoff frequency  $f_c$ . Between  $f_c$  and  $2 f_c$ , the filter must roll-off at the equivalent of at least 70 dB/octave. Above  $2 f_c$ , the filter response must remain at least 70 dB down from the passband.

In order to provide a well-defined set of filter/sampling characteristics, continuously variable cutoff frequencies and sampling rates will not be used. Rather, the available range of values will be covered roughly in octaves, each filter/sampling choice being approximately twice or half its neighbor. Table 2-7 shows the filter cutoff frequencies selected to go with Figure 2-17, together with the corresponding minimum input sampling rate, the sampling rate can be higher than that shown without degradation. However, aliasing may occur if a lower sampling rate is used. Note that at the highest,  $f_c = 4.5$  MHz setting, aliasing will occur if the original input spectrum is not down to  $< -60$  dB above 5 MHz.

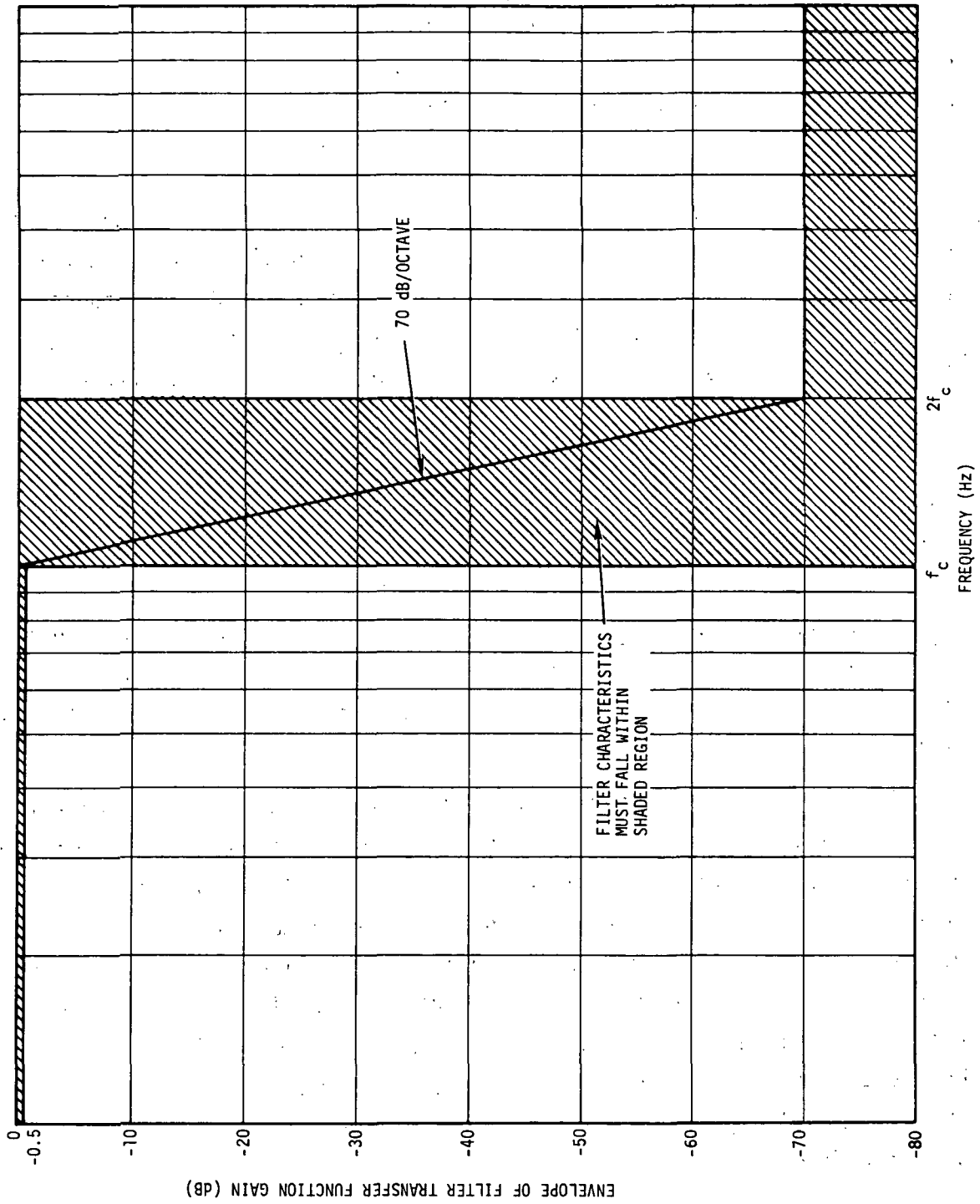


Figure 2-17. Universal Lowpass Filter Characteristics

Table 2-7. Filter Cutoff Frequencies and Associated Sampling Rates

Assumptions:  $f_{SR} = 4f_c$ , with at least 70 dB/octave filter rolloff above  $f_c$ .

Filter Cutoff Frequency $f_c$	Minimum A/D Converter Sampling Rate $f_{SR}$	Folding* Frequency $f_f = 0.5f_{SR}$
4.500 MHz	10.000 MHz	5.000 MHz **
2.500 MHz	10.000 MHz	5.000 MHz
1.250 MHz	5.000 MHz	2.500 MHz
625 KHz	2.500 MHz	1.250 MHz
320 KHz	1.280 MHz	640 KHz
160 KHz	640 KHz	320 KHz
80 KHz	320 KHz	160 KHz
40 KHz	160 KHz	80 KHz
20 KHz	80 KHz	40 KHz
10 KHz	40 KHz	20 KHz
5 KHz	20 KHz	10 KHz
2.5 KHz	10 KHz	5 KHz
1.25 KHz	5 KHz	2.5 KHz

\* To avoid aliasing, the combined signal and filter characteristics must yield a filter output signal that at frequencies above  $f_f$  is at least 70 dB down from the maximum level obtained at frequencies below  $f_c$ .

\*\* Suitable for color TV video only, which is down to < -60 dB at 5 MHz;  $f_{SR} = 2.222f_c$ .



### 2.3.6 Circuit Design

All units except the control logic and data buffer (Unit 5) are considered to be off-the-shelf equipment. Unit 5 most likely will be specially-procured. Thus, a more detailed functional description of this unit is required.

The functional make-up of Unit 5 is shown in Figures 2-18 and 2-19. The sample clock generator (Assembly 5A1) provides one of twelve precision "SAMPLE CLOCK" pulse trains (corresponding to the  $f_{SR}$  entries in Table 2-7), as determined by the "RATE SELECT" switch setting. The interrupt/acknowledge sequencer (Assembly 5A2) initiates each data acquisition cycle and conducts the initial dialog with the computer (Unit 6). The input-sample/buffer-load sequencer (Assembly 5A3) performs the sample-by-sample dialog with the A/D converter (Unit 4) and loads the converter output data words into the data buffer (Assembly 5A5). The data request/acknowledge sequencer (Assembly 5A4) shifts packed data words from the data buffer onto the data lines to the computer and conducts the word-by-word data-readout dialog with the computer. The data buffer (Assembly 5A5) stores data sample words until they have been transmitted to the computer.

#### 2.3.6.1 Assembly 5A1: Sample Clock Generator

The sample clock generator consists of a crystal oscillator, followed by a tapped binary counter. The "RATE SELECT" (Figure 2-18), or "SAMPLE RATE" (Figure 2-19), switch determines which of the counter output taps is used for the "SAMPLE CLOCK" signal. The sample rates provided by this assembly are listed in Table 2-7. The first three sample rates (2.5 MHz to 10 MHz) are generated using a 10,000 MHz crystal, while the remaining nine sample rates (5 kHz to 1.28 MHz) are generated using a 1.280 MHz crystal.

For sample rates 40 kHz and above (wideband configuration), the entire data buffer is used. For sample rates 20 kHz and below (narrowband configuration), only the final output buffer is used. Thus, in the wideband configuration, all data samples are converted and stored in the data buffer prior to readout to the computer. While in the narrowband configuration, each set of three consecutive data samples are transmitted to the computer as soon as the third sample has been loaded into the final output buffer.

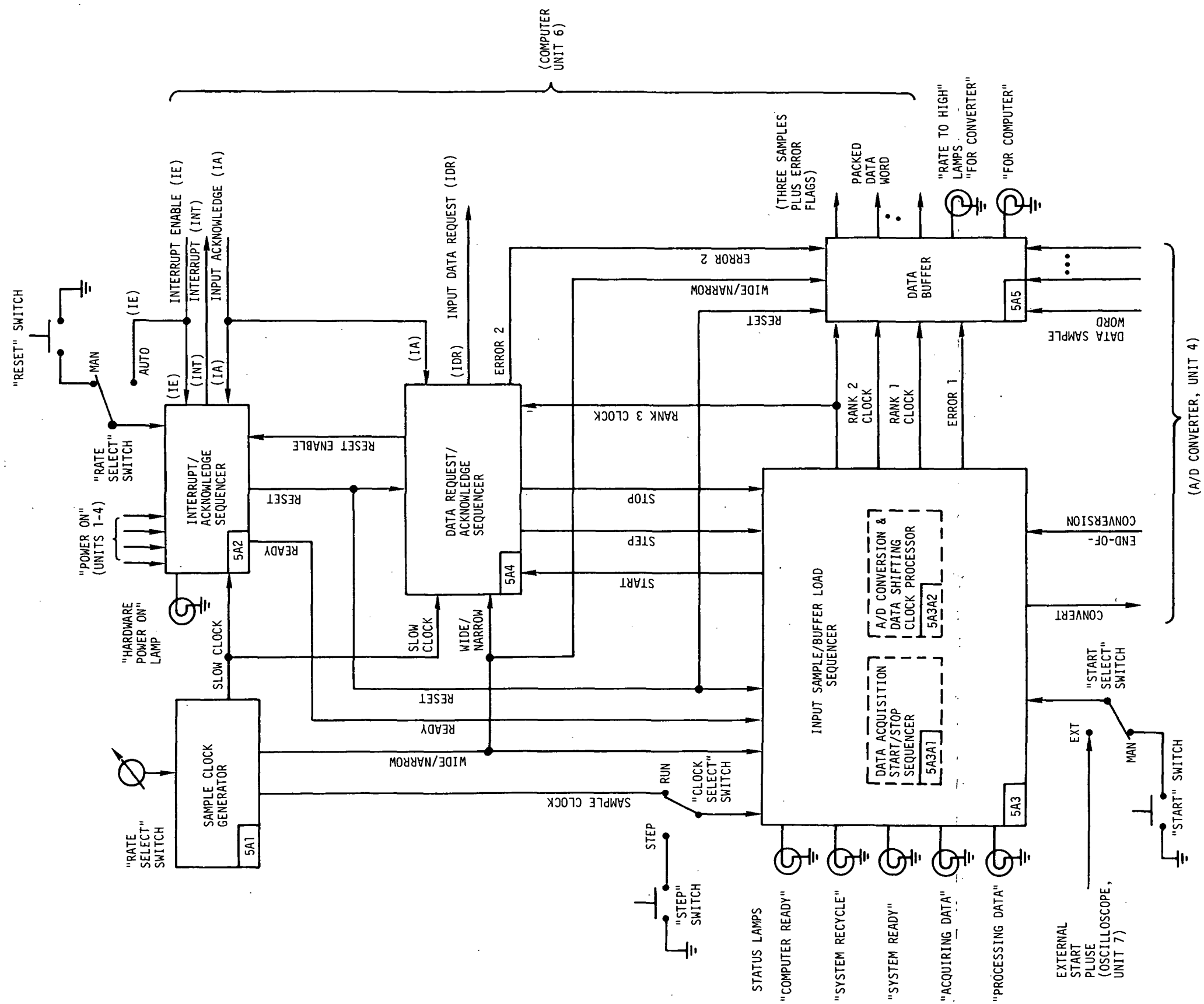
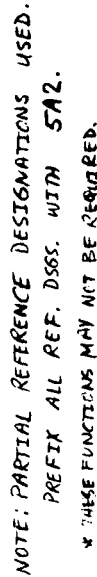
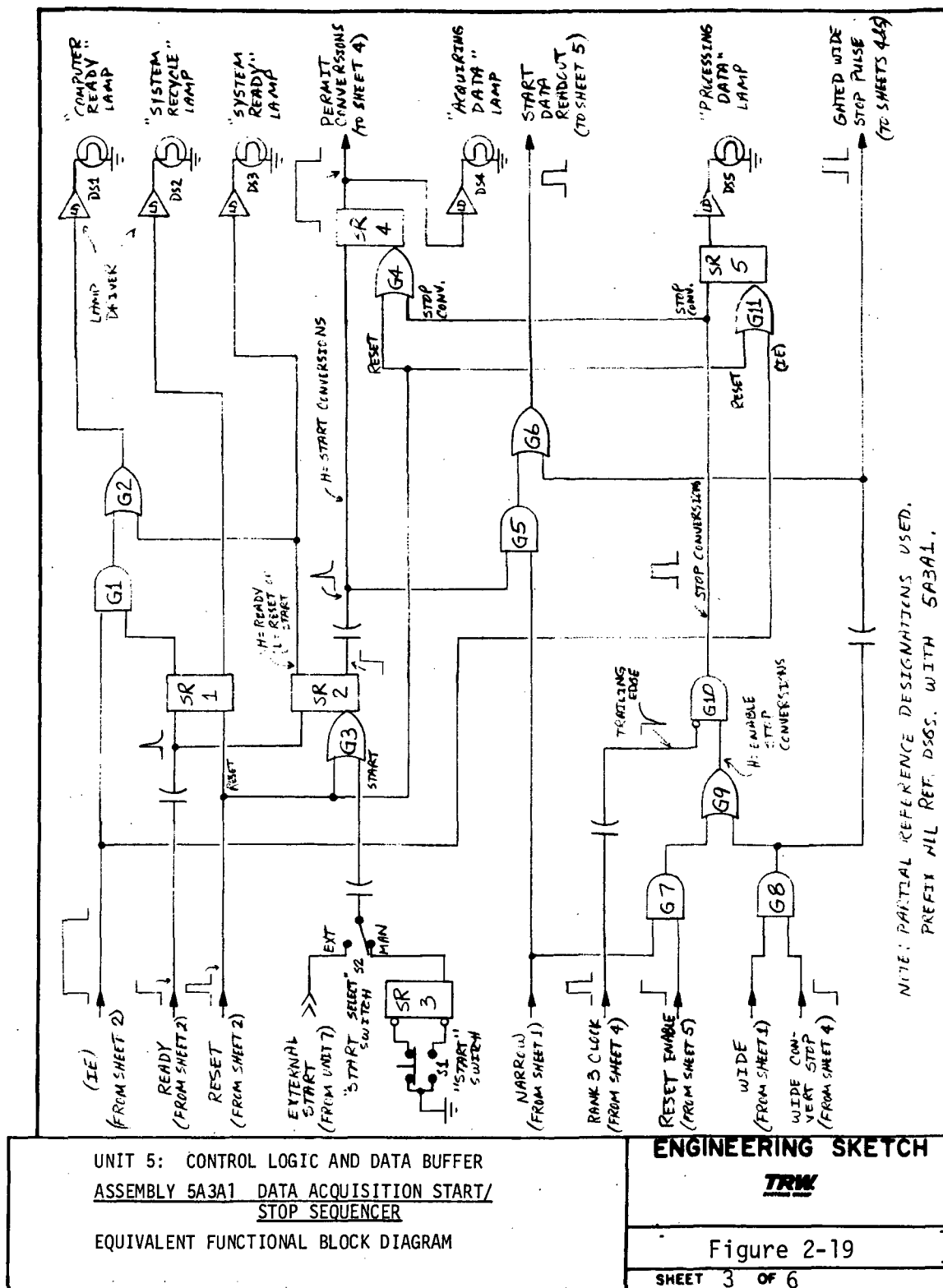


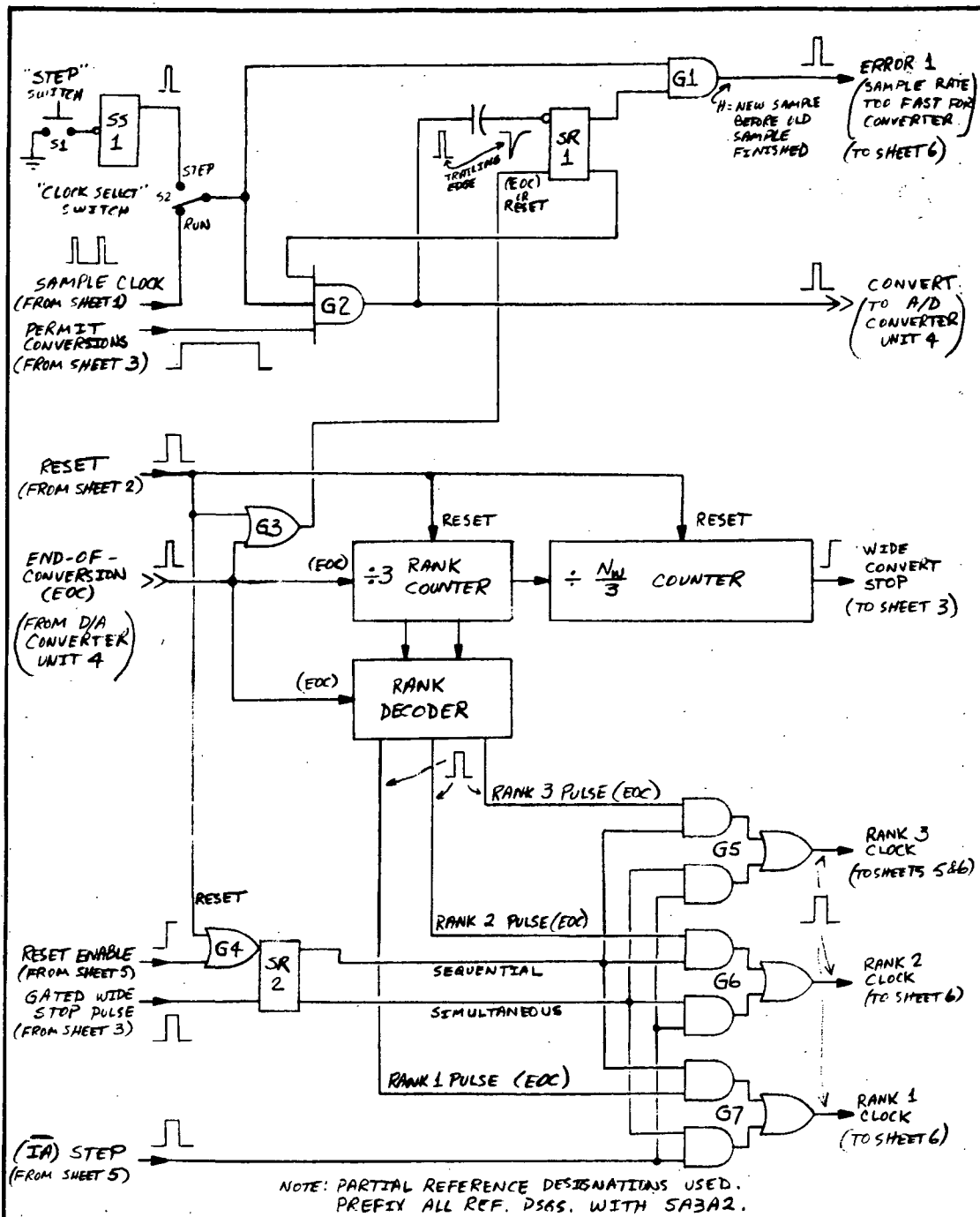
Figure 2-18. Data Acquisition Control Logic and Data Buffer





**SHEET 2 OF 6**





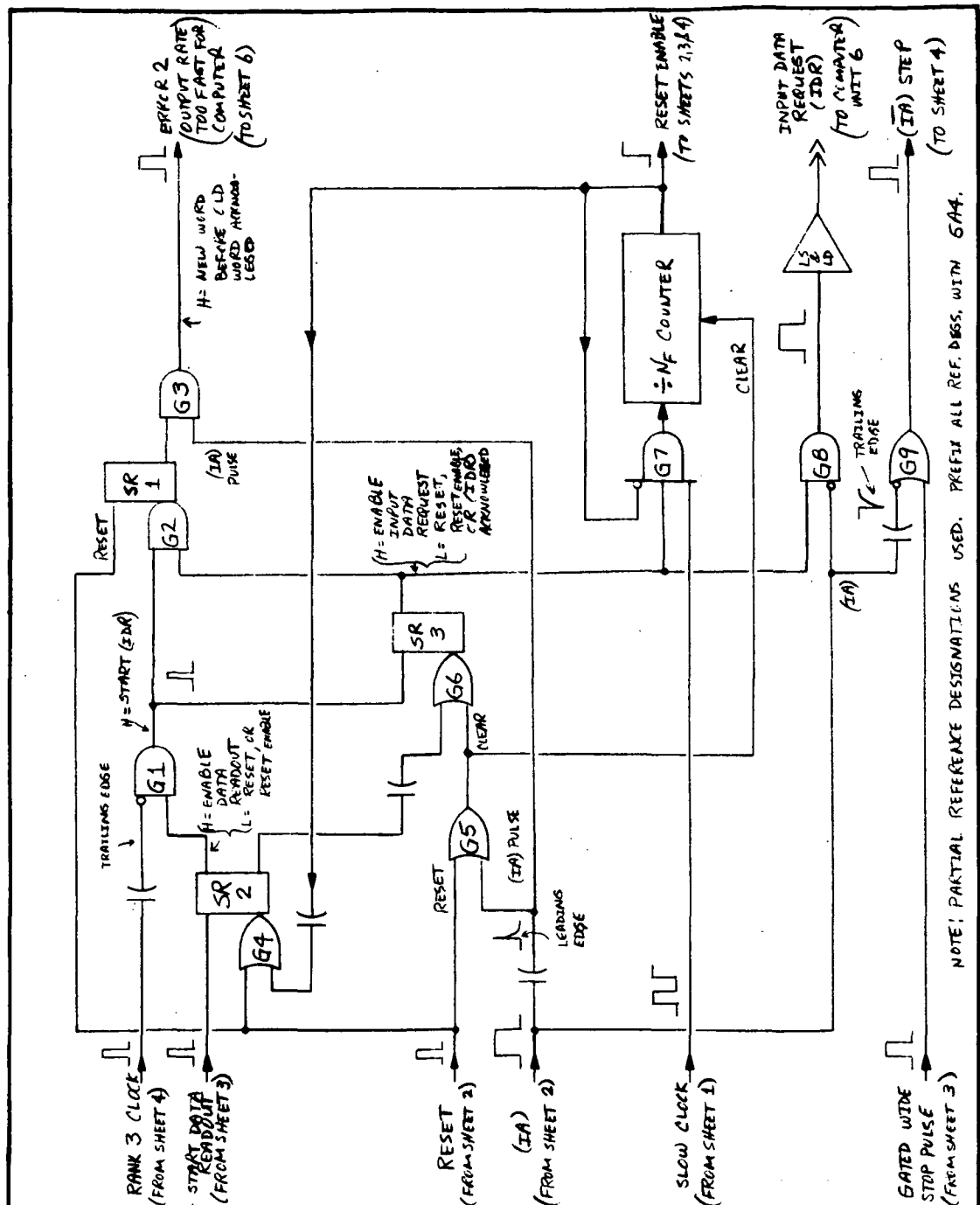
UNIT 5: CONTROL LOGIC AND DATA BUFFER  
ASSEMBLY 5A3A2 A/D CONVERSION AND DATA-  
SHIFTING CLOCK PROCESSOR  
 EQUIVALENT FUNCTIONAL BLOCK DIAGRAM

# ENGINEERING SKETCH

**TRW**

Figure 2-19

SHEET 4 OF 6



NOTE: PARTIAL REFERENCE DESIGNATIONS USED. PREFIX ALL REF. DES. WITH 6A4.

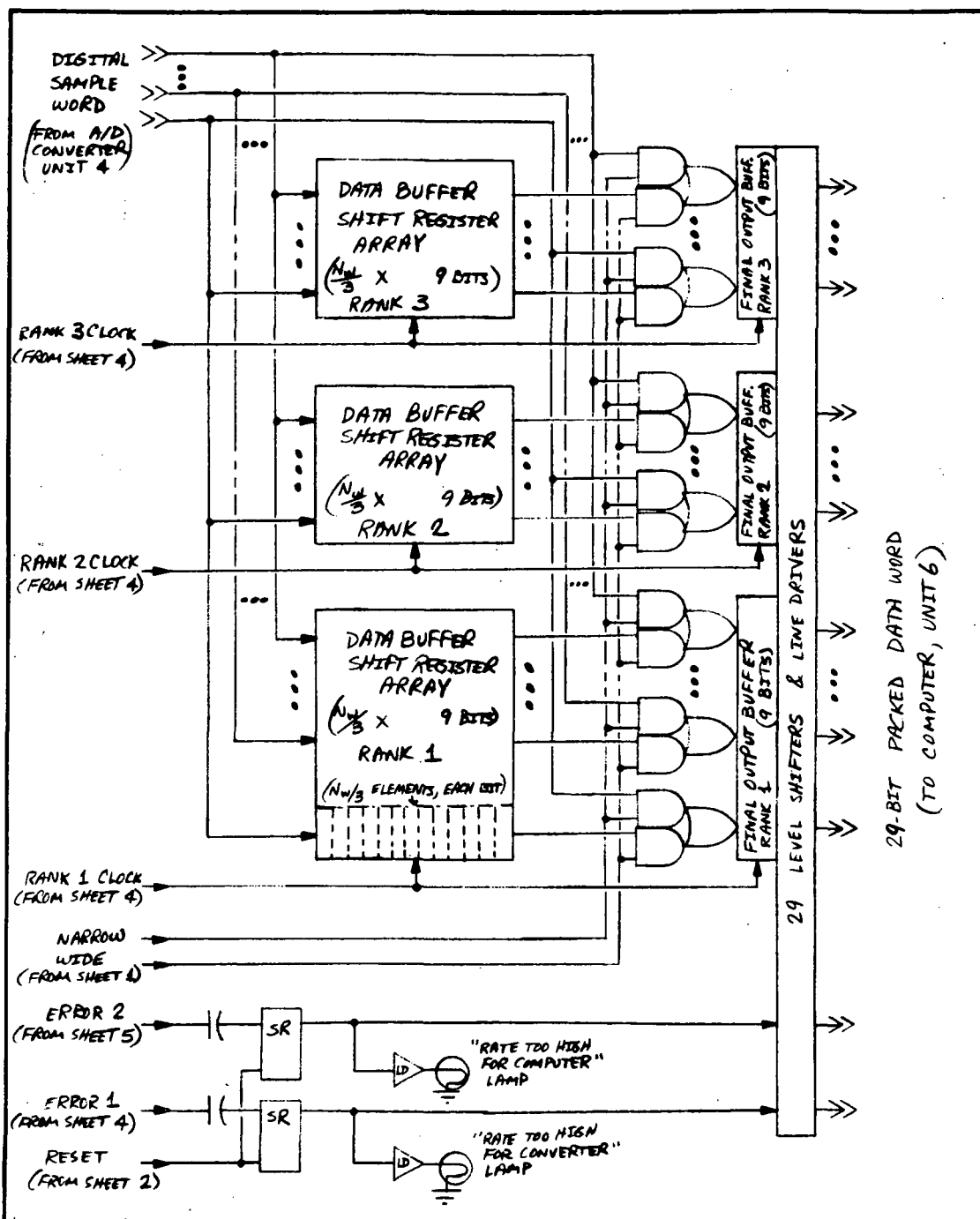
UNIT 5: CONTROL LOGIC AND DATA BUFFER  
 ASSEMBLY 5A4 DATA REQUEST/ACKNOWLEDGE  
 SEQUENCER  
 EQUIVALENT FUNCTIONAL BLOCK DIAGRAM

ENGINEERING SKETCH

TRW

Figure 2-19

SHEET 5 OF 6



UNIT 5: CONTROL LOGIC AND DATA BUFFER  
ASSEMBLY 5A5 DATA BUFFER  
EQUIVALENT FUNCTIONAL BLOCK DIAGRAM

ENGINEERING SKETCH

**TRW**

Figure 2-19

SHEET 6 OF 6



An equivalent functional block diagram of the sample clock generator is shown in Figure 2-19, Sheet 1. Even though schematic-like symbols are sometimes used, this and the following diagrams merely define the function of a circuit (not the schematic itself).

The "SAMPLE RATE" switch (the "RATE SELECT" switch in Figure 2-18) is shown as a 3-pole, 12-position rotary switch. The first pole (5A1S1A, or S1A for short) is used to connect either of the two crystals to the oscillator; for the first three positions, the 10 MHz crystal is used; for the remaining nine positions, the 1.28 MHz crystal is used. The second pole (5A1S1B, or S1B for short) is used to select the oscillator output (positions 1 and 4) or one of the binary counter output taps as the "SAMPLE CLOCK" signal source. The third pole (S1C) selects the wideband configuration (via gate G2) for the first nine settings (40 kHz to 10 MHz rates) or the narrowband configuration (via gate G3) for the remaining three settings (5 kHz to 20 kHz).

Gate G1 requires special description, since one of its inputs is shown as differentiating. The capacitor symbol represents differentiation in the functional sense that only the positive-going edge of the input signal enables gate G1. If the differentiation were omitted, the "SAMPLE CLOCK" signal would consist of bursts of oscillator pulses when the control input was at a logic "High (H)", and be a logic "Low (L)" when the control input was "L". With differentiation, however, the "SAMPLE CLOCK" signal consists of single oscillator pulses, occurring coincident with the leading edge of the control signal. In this manner, the "SAMPLE CLOCK" pulses always have the same shape, with the period of the pulses determined by the "SAMPLE RATE" switch setting.

#### 2.3.6.2 Assembly 5A2: Interrupt/Acknowledge Sequencer

The interrupt/acknowledge sequencer, Figure 2-19, Sheet 2, consists of gates and flip-flops which are used during initialization of a data acquisition cycle. As before, this diagram is functional and is not intended to be a circuit or logic diagram. The gate symbols, drawn according to

MIL-STD-806, represent "AND" functions (G1 through G5, and G8) or "OR" functions (G6, G7, and G9). The flip-flop symbols represent "SET-RESET" functions (SR1 through SR3) and "J-K" functions (JK1).

A "SET-RESET" or "SR" flip-flop is an asynchronous memory device that enters the "SET" state (upper output "H" and lower output "L") when its upper input is pulsed "L"→"H"→"L" and enters the "RESET" state (upper output "L" and lower output "H") when its lower input is pulsed; undefined operation occurs if both inputs are pulsed simultaneously. As used here (see JK1), and "J-K" flip-flop is a synchronous memory device which operates as a  $\div 2$  counter.

Starting with gates 5A2G7, 5A2G8, and 5A2G9 (or G7, G8, and G9 for short) and flip-flop SR3, the control logic is forced into a known initial condition by the power turn-on reset circuit, which applies a reset pulse to all flip-flops (via G9) whenever the logic power is first energized. Otherwise, the logic cannot be reset unless enabled from the data request/acknowledge sequencer ("RESET ENABLE"). Occurring after all acquired data samples have been transmitted to the computer, "RESET ENABLE" allows gate G8 to accept a reset input. If the "RESET MODE" switch S2 ("RESET SELECT" in Figure 2-18) is in the "MAN" position, reset occurs only when the "RESET" pushbutton S1 is depressed. If "AUTO" has been selected, reset occurs upon receipt of "INTERRUPT ENABLE" (IE) from the computer. The reset signal from G8 to G9 is differentiated, to assure that "RESET" is a narrow pulse.

In the reset condition, the upper output of flip-flop SR1 is "H" and the lower output is "L", the lower output of JK1 is "H", and the upper output of SR2 is "L". Thus, G2 is enabled by SR1, G4 is enabled by JK1, and G5 is disabled by SR2.

When Units 1 through 4 are turned "ON", G1 is activated, enabling G2 and lighting the "HARDWARE ON" lamp 5A2DS1. If the "INTERRUPT ENABLE" (IE) signal becomes active while the logic is reset and the hardware power is on, G2 is activated, thereby activating G4 and raising the "INTERRUPT" (INT) line. While G2 is activated, G3 allows "SLOW CLOCK" pulses to trigger JK1, which periodically permits and inhibits G4. Consequently, (INT) is a

pulsed signal which is approximately a 2.5 kHz square wave. Note that, if the computer cannot properly handle pulsed interrupts, gates G3 and G4 and flip-flop JK1 can be omitted, leaving the output of G2 as the (INT) signal. In this case, (INT) remains active until SR1 is pulsed by G5.

When the first (INT) occurs, SR2 is pulsed into the "SET" state, enabling G5. At this point no further action other than pulsed or steady (INT) signals occur until the simultaneous occurrence of a raised "INPUT ACKNOWLEDGE" (IA) and a dropped (IE) from the computer. This simultaneous event indicates that the computer has honored the interrupt, has initialized its input buffer, and is acknowledging the interrupt.

When the interrupt is acknowledged, G5 pulses SR1 and SR2. SR2 promptly disables G5, so that subsequent (IA) signals will be ignored. SR1 disables G2, so that no further interrupts will be generated. SR1 activates the "READY" signal, to indicate that the computer has configured to accept input data words.

#### 2.3.6.3 Assembly 5A3: Input Sample/Buffer Load Sequencer

The sample/load sequencer is divided into two subassemblies (5A3A1: Data Acquisition Start/Stop Sequencer, Figure 2-19, Sheet 3, and 5A3A2: A/D Conversion and Data-Shifting Clock Processor, Figure 2-19, Sheet 4). The start/stop sequencer (Sheet 3) controls the start and stop of both the A/D conversion sampling and the data readout to the computer. The clock processor (Sheet 4) counts each conversion as it is completed and activates the appropriate clock signal for loading the data sample into the data buffer.

Starting with Sheet 3, gates 5A3A1G1 and 5A3A1G2 and flip-flops 5A3A1SR1 and 5A3A1SR2 (or G1, G2, SR1, and SR2 for short) determine in which of several operational modes the system exists. For example, if the system has completed a data acquisition cycle, the "INTERRUPT ENABLE" (IE) signal will be raised. If manual reset has been selected via switch 5A2S2, and if the manual reset button 5A2S1 has not been depressed, then SR1 will

remain "SET", and the "COMPUTER READY" lamp 5A3A1DS1 will be lighted, via G1 and G2. This lighted lamp can be used by the operator as a cue for operating the manual reset.

Once reset has been activated, SR1 and SR2 are "RESET", and the "SYSTEM RECYCLE" lamp DS2 becomes lighted, to indicate that the interrupt/acknowledge computer buffer-initiation dialog is in progress; DS1 is "OFF". When this process is completed, (IE) is dropped and "READY" is activated. SR1 and SR2 are "SET", lighting the "SYSTEM READY" lamp, DS3, and the "COMPUTER READY" lamp, DS1, via G2; DS2 is "OFF". Depending on the setting of the "START SELECT" switch 5A3A1S2, SR2 waits for a start pulse either from an external trigger, or from the "START" switch 5A3A1S1. If S2 is in the "MANUAL" position, the operator can use the lighted lamp DS3 as a cue to depress pushbutton S1.

Following the "START" pulse, SR2 is "RESET", via G3, turning off DS1 and DS3. The rising edge of SR2's lower output is differentiated, pulsing SR4 and lighting the "ACQUIRING DATA" lamp DS4. If the narrowband configuration has been selected (20 kHz or lower sampling rate), the "NARROW" signal is active, and the SR2 pulse is gated through G5 and G6 to start readout of data to the computer. In this case, conversions and data readout continue until the "RESET ENABLE" signal enables G10 via G7 and G9. At the trailing edge of the next "RANK 3 CLOCK" pulse, G10 pulses SR4 and SR5. Subsequent conversions and inputs to the computer are stopped, DS4 is extinguished, and the "PROCESSING DATA" lamp DS5 is lighted, to indicate that the computer is working with the data previously transmitted to its input buffer. When the computer is finished writing formatted samples on the tape, (IE) is raised, turning on DS1 and extinguishing DS5.

If, on the other hand, the wideband configuration has been selected (40 kHz or higher sampling rate), all data samples are acquired and stored in the data buffer prior to any readout to the computer. In this case, overflow of the data sample counter ("WIDE CONVERT STOP" going "H") disables further A/D sampling via G8, G9 and G10, while data readout to the computer is enabled via G8, and G6.

Continuing with Figure 2-19; Sheet 4, the "CLOCK SELECT" switch 5A3A2S2 (or S2 for short) selects whether the A/D converter is to be clocked by the "SAMPLE CLOCK" pulses or by the operator depressing the "STEP" switch S1. If the "STEP" mode has been selected, single shot SS1\* pulses every time S1 is actuated, generating a single clock pulse. This mode is provided primarily as a system test function, enabling the operator to acquire each data sample manually.

Under normal operating conditions, the "PERMIT CONVERSIONS" signal from 5A3A1SR4 enables "SAMPLE CLOCK" pulses to propagate through 5A3A2G2 (or G2 for short), becoming "CONVERT" commands for the A/D converter. Every time a convert command is given, SR1 is pulsed. If a subsequent clock pulse occurs before an "END-OF-CONVERSION" (EOC) pulse is received (for the previous clock pulse), G1 pulses to indicate that the input sampling is running too fast for the converter; SR1 blocks further new clock pulses via G2, unless and until an (EOC) is received.\*\*

Assuming that the sample rate is within the converter's capability, each convert command pulse is acknowledged by an (EOC) pulse. As each (EOC) is received, the "RANK COUNTER" and "DECODER" distribute this (EOC) pulse via G5, G6, or G7 to the clock input of one of three storage arrays or ranks within the data buffer (SR2 is initially in the "SEQUENTIAL" mode). The first (EOC) clocks Rank 1, the 2nd: Rank 2, the 3rd: Rank 3, the 4th: Rank 1, the 5th: Rank 2, etc. Since gate 5A3A1G10 allows conversion and loading of data samples to cease only at the end of the "RANK 3 CLOCK" pulse, data acquisition always terminates with the three data ranks properly aligned or all filled to the same depth. Thus, input samples are always processed in groups of three.

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\* Single-shot flip-flops are also known as one-shots or monostable multi-vibrators.

\*\* This feature allows any of several types of converter to be used as Unit 4. Erroneous data samples are thereby avoided should a sample rate too high for the converter be selected.

In the wideband configuration, conversions are terminated when all ranks have been filled. At this time, SR2 is pulsed to the "SIMULTANEOUS" mode (via the "GATED WIDE STOP PULSE"), enabling " $\overline{(IA)}$  STEP" pulses to clock all ranks at the same time, via gates G5, G6, and G7. SR2 is returned to the "SEQUENTIAL" mode at reset time.

#### 2.3.6.4 Assembly 5A4: Data Request/Acknowledge Sequencer

The data request/acknowledge sequencer, Figure 2-19, Sheet 5, is inactive until the "START DATA READOUT" pulse (from gate 5A3A1G6) is received. In the narrowband mode, this pulse occurs as soon as the A/D conversions are started; in the wideband mode, this pulse occurs after all input data samples have been stored in the data buffer. Flip-flop 5A4SR2 (SR2) is set by this pulse, allowing the trailing edge of the "RANK 3 CLOCK" pulses to set SR3 via G1.

Provided that the "INPUT ACKNOWLEDGE" (IA) signal from the computer is not active, the state of SR3 becomes via G8 the "INPUT DATA REQUEST" (IDR) signal to the computer.\* If a subsequent "RANK 3 CLOCK" pulse should occur before an (IA) pulse resets SR3, SR1 is pulsed via G2. If an (IA) pulse occurs after SR1 is armed, G3 pulses to indicate that the computer is not accepting data words fast enough; in this event, one or more 3-sample words may have been lost.

While the (IDR) is active, the  $N_F$  counter is incremented by the "SLOW CLOCK" signal via G7;  $N_F$  is the number of number of "failures to receive an (IA)" following the activation of (IDR). The  $N_F$  counter is used to terminate the data readout sequence if the computer stops acknowledging input data requests. Note that this is the normal termination mode, so G3 does not pulse an error condition indication in this case, since no subsequent (IA) pulse is received.

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\* This assumes that (IA) is dropped when the computer senses that (IDR) has dropped.

During data readout, if the (IDR) is acknowledged with an (IA), SR3 is reset via G5 and G6, and the  $N_F$  counter is cleared via G5. The (IDR) is dropped, and nothing further happens until the trailing edge of the next "RANK 3 CLOCK" pulse activates the next (IDR).

Gate G9 provides " $\overline{(IA)}$  STEP" pulses for use as a parallel readout clock signal when the system is in the wideband configuration. These pulses clock the data buffer after it has been filled with input sample words. The first such pulse is derived from the "GATED WIDE STOP" pulse, since an (IA) is received only after (IDR) has been activated. All subsequent pulses are derived from the trailing (falling) edge of the "INPUT ACKNOWLEDGE" (IA) signal.\* With this approach, the transfer of data to the computer is at the maximum achievable rate, since a new (IDR) is sent as soon as the previous (IA) is dropped by the computer.\*\*

#### 2.3.6.5 Assembly 5A5: Data Buffer

The data buffer, Figure 2-19, Sheet 6, provides for direct readout of input sample words to the computer (narrowband mode) by sequentially loading three 9-bit A/D converter output words directly into the (double-buffered) final output buffer. The first sample word is loaded into the Rank 1 buffer at "RANK 1 CLOCK" time, the second sample into the Rank 2 buffer at "RANK 2 CLOCK" time, and the third sample into the Rank 3 buffer at "RANK 3 CLOCK" time. At the end of the "RANK 3 CLOCK" pulse, the initial contents of the final output buffer are transferred to the holding or second portion of the final output buffer (placing the data on the input lines to the computer), the (IDR) signal is activated, and the computer reads the resultant, packed 29-bit (27-bit sample data plus 2-bit error flag) data word. This conversion/readout process is continued in groups of three input samples until the computer terminates the operation by not acknowledging the last (IDR).

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\* This assumes that (IA) is dropped when the computer senses that (IDR) has dropped.

\*\* This also assures that the minimum timing requirements of the computer are satisfied, without the need for delays in the control logic.

For wideband operation, each 9-bit A/D converter output word is loaded into a shift-register array. The shift-register storage is organized into three ranks of 9 bits each, for a total of 27 parallel shift registers, each  $N_w/3$  bits long, where  $N_w$  is the number of wideband samples to be stored. Each bit of the first sample word is loaded into the first stage of the corresponding shift register in Rank 1, the second sample is loaded into Rank 2, the third into Rank 3, the fourth into Rank 1, the fifth into Rank 2, etc. As a new word is loaded into a given shift-register rank, the previous contents in that rank are shifted down one stage into the rank. As a result, the word-to-word sequence within Rank 1 is always data samples 1, 4, 7, 10, 13, 16, etc., while the corresponding contents of Rank 2 is always data samples 2, 5, 8, 11, 14, 17, etc., and Rank 3 always contains data samples 3, 6, 9, 12, 15, 18, etc. After the "RANK 3 CLOCK", similarly-numbered stages within the three ranks are always loaded with data sample words in the order 1-2-3, 4-5-6, 7-8-9, 10-11-12, 13-14-15, 16-17-18, etc.

As the wideband input samples are being acquired, the three rank clocks operate sequentially, as for the narrowband mode. When all input sample words have been stored, the conversion process is halted and the three clocks are strobed simultaneously, shifting composite 27-bit packed data words into the (single-buffered) final output buffer. As each new data word is placed onto the input lines to the computer, the (IDR) signal is activated, and the computer reads the resultant, packed data word, as in the narrowband case. Data readout to the computer is terminated as in the narrowband case.

The exact organization of the data buffer assembly can be better understood in terms of a specific example. The maximum number of data samples which can be conveniently processed by the spectral analysis program is 16,384. This limitation is partially due to storage limits within the computer but is primarily due to the very long floating point multiplication times involved.\* The nearest grouping of three to this number of samples is

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\* There is no floating point hardware in the computer being specified, so the multiplications are accomplished with software using the integer hardware. Typical multiplication times are said to be of the order of 900  $\mu$ sec.



16,386, which corresponds to three storage ranks each of length 5462. If the shift register elements are available in lengths up to 1024 bits each, the required data buffer storage, including final output buffer, is 27 parallel groups (i.e., three sets of 9 bits each) of five 1024-bit shift registers, one 341-bit shift register, and one 2-bit (final output buffer) shift register, all connected "head-to-tail" in series ( $5120 + 341 + 2 = 5462 + 1$ ). The first 5461 bits can be provided by MOS-type dynamic shift register elements, while the remaining two bits most probably should be bipolar (e.g., TTL) elements.

The maximum wideband input sampling rate is 10 MHz, so the maximum shift rate in any shift register within the data buffer is 3.333 MHz, well within the current capabilities of MOS shift-register technology. The minimum input sampling rate for the wideband configuration is 40 kHz, so the minimum shift rate for any shift register in the data buffer is 13.33 kHz, also well within the current technology for dynamic MOS shift-register memories. The maximum narrowband input sampling rate is 20 kHz, so the maximum clocked input rate to the computer is 6.667 kHz, almost two orders of magnitude below the nominal maximum that the computer can accept. The minimum input sampling rate for the narrowband configuration is 5 kHz, so the minimum input rate to the computer is 1.667 kHz.

Based on the acquisition of 16,386 data samples, Table 2-8 shows the length of the time record processed for each of the input sampling rates in Table 2-7, plus the approximate time for transferring the data samples to the computer, assuming an average maximum transfer rate of 100 kHz. At a 15.75 kHz TV scan frequency, each TV scan line is 63.5  $\mu$ sec. long (from the beginning of one scan line to the beginning of the next). At a 10 MHz sampling rate, there will be 635 samples/line, so 16,386 samples correspond to 25.8 scan lines.

Table 2-8. Data Acquisition and Computer Input Times

Assumptions: 16,386 input samples, 100 KHz average  
max. input rate to computer

Input Sampling Rate (MHz)	A/D Conversion Acquisition Time (msec)	Additional Computer Input Time (msec)	Total Acquisition Time (msec)
10.000	1.6385	163.86	165.5 +
5.000	3.2770	163.86	167.1 +
2.500	6.5540	163.86	170.4 +
1.280	12.801	163.86	176.7 +
0.640	25.602	163.86	189.5 +
0.320	51.203	163.86	215.1 +
0.160	102.41	163.86	266.3 +
0.080	204.82	163.86	368.7 +
0.040	409.63	163.86	573.5 +
0.020	819.25	-	819.3 +
0.010	1638.5	-	1639 +
0.005	3277.0	-	3277 +

### 3. CONCLUSIONS AND RECOMMENDATIONS

The Spectral Analysis Program described in this report provides NASA/ MSC with a capability for performing spectral analysis of a wide variety of the angle modulated signals likely to be transmitted in an angle modulated communication system. The internal test signals supplied as an integral part of the program permit the spectrum produced by many commonly encountered modulating signals to be evaluated directly without the need for external hardware to provide input data. When the modulating signal is not one of those supplied by the internal test signal generator the necessary input data can be provided by the data acquisition system whose design is described in this report. The data acquisition system will acquire data at rates up to  $10^7$  samples/second. When operated under the control of the UNIVAC 1230 computer, this system will automatically sample the input data, convert the sampled data to digital words, transfer these words to the UNIVAC 1230 computer and prepare a magnetic tape with the data in the proper format for use as input data to the Spectral Analysis Program.

The computational approach used in the SAP is to form the angle modulated signal as a time domain function and then compute its spectrum by means of the Fourier transform. This technique is effective for essentially arbitrary modulating signals and is efficient with respect to program running time. The success of the direct Fourier transform approach is due in large measure to the use of the Extended Fast Fourier Transform (EFFT) algorithm which was developed under this contract for the SAP program. The EFFT provides the ability to compute the Fourier Transform of the very large data arrays needed to adequately represent many practical modulating signals.

The SAP program provides a direct means of assessing the effects of signal processing in angle modulation transmitters. This capability should be expanded to include the ability to evaluate the effects of receiver processing in angle modulation receivers. What is needed is a new computer

program which will evaluate the effects of filtering, frequency translation, limiting, and demodulation on angle modulated signals and provide a time function plot of the demodulated output signal. The input requirements of the new program should be compatible with the output of the SAP program. These two programs, when operated in cascade, would provide a capability for assessing performance degradation caused by both transmitters and receivers in an angle modulated transmission system.

## APPENDIX A

### 1.1 THE EXTENDED FAST FOURIER TRANSFORM

#### THE DISCRETE FOURIER TRANSFORM

Both the Fast Fourier Transform (FFT) and the Extended Fast Fourier Transform (EFFT) algorithms compute the discrete Fourier transform or its inverse for a given signal. The discrete Fourier transform pair is defined by

$$X(j) = \frac{1}{N} \sum_{k=0}^{N-1} x(k) W_N^{-jk} \quad (A-1)$$

$$x(k) = \sum_{j=0}^{N-1} X(j) W_N^{jk} \quad (A-2)$$

for  $j=0, 1, \dots, N-1$  and  $k=0, 1, \dots, N-1$ .  $W_N$  is defined by

$$W_N = \exp(2\pi i/N) \quad (A-3)$$

where  $i = \sqrt{-1}$ .

In the above  $x(k)$  represents the time-domain function and  $X(j)$  represents the frequency-domain function.

Consider the expression

$$\hat{x}(j) = \sum_{k=0}^{N-1} A(k) W_N^{jk} \quad (A-4)$$

By comparison with Equations (A-1) and (A-2)

$$\text{if } A(k) = \frac{x^*(k)}{N} \quad \text{then } \hat{x}(j) = \hat{x}^*(j)$$

and if

$$A(k) = X(j) \quad \text{then } \hat{x}(j) = x(k)$$

where the \* superscript denotes the complex conjugate. Thus, only Equation (A-4) needs to be considered in computing Equations (A-1) and (A-2).

#### ALGEBRA OF THE EFFT

Suppose N, in Equation (A-4), may be written as

$$N = LM$$

where both M and L are powers of 2.

The indices j and k in Equation (A-4) may be expressed as

$$k = l + mL$$

$$j = m' + l'M$$

where  $l = 0, 1, \dots, L - 1$ ;  $m = 0, 1, \dots, M - 1$ ;  $m' = 0, 1, \dots, M - 1$ ;  
and  $l' = 0, 1, \dots, L - 1$ .

In terms of the new indices Equation (A-4) becomes

$$x(m' + l'M) = \sum_{l=0}^{L-1} \sum_{m=0}^{M-1} A(l + mL) W_N^{(m'+l'M)(l+mL)} \quad (A-5)$$

Now

$$\begin{aligned} W_N^{(m'+l'M)(l+mL)} &= \exp\left[\frac{2\pi i}{N} (m'+l'M)(l+mL)\right] \\ &= \exp\left[2\pi i\left(\frac{m'l}{N} + \frac{l'l}{L} + \frac{m'm}{M} + l'm\right)\right] \\ &= W_N^{m'l} W_L^{l'l} W_M^{m'm} W_1^{l'm} \end{aligned}$$

the term  $w_1^{1'm} = 1$ .

So Equation (A-5) becomes

$$x(m'+1'M) = \sum_{l=0}^{L-1} \sum_{m=0}^{M-1} A(1+mL) w_N^{m'1} w_L^{1'1} w_M^{m'm} \quad (A-6)$$

Rewriting Equation (A-6) as

$$\hat{x}(m'+1'M) = \sum_{l=0}^{L-1} w_N^{m'1} w_L^{1'1} \sum_{m=0}^{M-1} A(1+mL) w_M^{m'm} \quad (A-7)$$

In Equation (A-7) define  $A_1(m',1)$  by

$$A_1(m',1) = \sum_{m=0}^{M-1} A(1+mL) w_M^{m'm} \quad (A-8)$$

Comparing Equations (A-8) and (A-4), then  $A_1(m',1)$  is the discrete Fourier transform evaluated at index or frequency  $m'$  of the series produced by taking every  $L^{\text{th}}$  sample from  $A$ . These samples are produced by beginning from the  $1^{\text{th}}$  sample of  $A$ . There are  $L$  of the sequences  $A_1(m',1)$ , each has  $M$  terms.

Defining

$$\begin{aligned} &\hat{A}(m',1) \text{ by} \\ &\hat{A}(m',1) = w_N^{m'1} A_1(m',1) \end{aligned} \quad (A-9)$$

and substituting into Equation (A-7) yields

$$\hat{x}(m'+1'M) = \sum_{l=0}^{L-1} A(m',1) w_L^{1'1} \quad (A-10)$$

Comparing Equations (A-10) and (A-4) indicates that  $\hat{x}$  is produced by taking the discrete Fourier transform of the M sequences defined by Equation (A-9).

All FFT transform algorithms are based upon factoring N into products and then going through algebra steps as above. The algorithm used as a subroutine in the EFFT routine is based upon factoring N into products of 2.

#### MATRIX INTERPRETATION

The algebra of the EFFT has a simple interpretation in terms of matrices. Consider the original signal term  $A(1 + mL)$  in Equation (A-5). The  $l, m$  indexing is such that A may be stored as a complex matrix with M rows and L columns. Thus, m is the row index and l is the column index. The discrete Fourier transforms defined by Equation (A-8) represent the separate transforms of each column of the matrix. There are L such columns and each is of length M. After transforming, the complex array represented by  $A_l(m', l)$  is stored as a matrix with  $m'$  representing the row index and l the column index.

The operation defined by Equation (A-9) represents multiplying each term of the resulting transforms by an appropriate  $\cos + i \sin$  terms. This complex sinusoidal term is called the "twiddle factor."

The discrete Fourier transform defined by Equation (A-10) is produced by transforming separately each row of the complex matrix A. There are M rows and each row has L terms. The row index is  $m'$  and the column index is  $l'$ .

#### DETAILS OF THE EFFT ALGORITHM

In order to transform extremely long data sequences, the EFFT routine that has been implemented uses tapes for storage of the input and output signals. Two tapes are required.

The matrix interpretation of the previous section indicates that the general flow of the algorithm must be

1. The data is input, properly stored as a complex matrix on tape 1.
2. Transform each column of the matrix on tape 1 and multiply by the twiddle factor and store on tape 2.



3. Transpose complex matrix on tape 2 and store on tape 1.
4. Transform each column of the matrix on 1 and store final result on tape 2.

The transpose is required as the algebra indicates than in the first set of transforms the columns are operated on while in the second set of transforms the rows are operated on.

The format of the data on the tapes at input or output is as follows: Let  $AR(I,J)$  and  $AI(I,J)$  denote the real and imaginary components of the complex matrix respectively. The index  $I$  corresponds to the row index where  $I=1, \dots, NR$ . The index  $J$  corresponds to the column index where  $J=1, \dots, NC$ . Then the matrices  $AR$  and  $AI$  are stored on the tape as

Record 1	$AR(I,1)$	$I = 1, \dots, NR$
Record 2	$AI(I,1)$	$I = 1, \dots, NR$
Record 3	$AR(I,2)$	$I = 1, \dots, NR$
Record 4	$AI(I,2)$	$I = 1, \dots, NR$
.		
.		
.		
Record $2*NC-1$	$AR(I,NC)$	$I = 1, \dots, NR$
Record $2*NC$	$AI(I,NC)$	$I = 1, \dots, NR$

If at input the row and column dimensions are  $NR = NR1$  and  $NC = NC1$ , then at output the row and column dimensions are  $NR = NC1$  and  $NC = NR1$ . This interchange of the dimensions of the  $AR$  and  $AI$  arrays is due to the transpose operation.

The correspondence between the  $(I,J)$  indices and the time or frequency variables at either input or output is as follows:

- A. If  $AR$  and  $AI$  represent the real and imaginary parts of a time function, then the value of the time variable  $t$  is

$$t = [(j-1) + NC*(I-1)]*\Delta t$$

for  $J = 1, \dots, NC$  and  $I = 1, \dots, NR$  and where  $\Delta t$  is the time separation between points.

B. If AR and AI represent the real and imaginary parts of a frequency function, then the value of the frequency variable  $f$  is

1. For  $I = 1, NR/2$

$$f = [(J-1) + (I-1)*NC]*\Delta f$$

for  $J = 1, \dots, NC$  and where  $\Delta f$  is the frequency separation between points, i.e.,

$$\Delta f = \frac{1}{NR*NC*\Delta t}$$

2. For  $I = (NR/2) + 1, NR$

$$f = -[(NR*NC-(J-1)-(I-1)*NC]*\Delta f$$

for  $J = 1, \dots, NC$ .

## APPENDIX B

### DATA ACQUISITION SYSTEM SPECIFICATIONS

Specifications for each element of the data acquisition system, outlined in Figures 2-14, 2-18, and 2-19, and described in the paragraph 2.3, are given in the following paragraphs. Units 1 through 4, and 7, the signal source, lowpass filter, scaling amplifier, and (optional) oscilloscope and/or peak-reading voltmeter, respectively, are treated as off-the-shelf components. The unit 5 control logic and data buffer is specified as a specially-manufactured component. The unit 6 computer is assumed to be the UNIVAC 1230 or equivalent, e.g., the UNIVAC CP-642B/USQ-20(V). The required data acquisition software program is specified by a flow diagram.

#### General Specifications

All units must meet the following general specifications. The complete specifications for a particular unit will consist of these general specifications, plus the specifications unique to that unit.

##### 1. Environmental

- a. Operating temperature: 0° to 50°C ambient
- b. Storage temperature: -20° to +85°C
- c. Humidity: 1° to 90° RH without condensation
- d. Shock and Vibration: Normal transportation
- e. Warm-Up: 15 minutes maximum

##### 2. Mechanical

###### a. Size and Mounting

- 1) Nineteen inch rack-mountable (except computer), plus front-panel mountable (except computer)
- 2) Chassis slides (tilting or nontile type) included (except computer)

- 3) Maximum Height: 10 inches
  - 4) Maximum Depth: 30 inches
  - b. Controls and Displays (indicators)
    - 1) Accessible from the front
    - 2) Remote programming capability provided
  - c. Signal and Power Connections
    - 1) AC Power: 3-wire grounding
    - 2) Remote Programming Signals: Suitable multi-pin connectors
    - 3) Computer/Logic Signals: Multi-pin connector compatible with computer interface requirements
    - 4) All other signals: BNC connectors
  - d. General: Each unit shall be manufactured to good commercial product standards
  - e. Manuals: Two copies of instruction manuals will be furnished for each unit. These manuals will be accurate to the equipment as furnished and will include:
    - 1) Theory of Operation
    - 2) Schematic and Logic Diagrams, including diagrams for non-standard components or modules
    - 3) Wiring Diagrams, with all circuit components shown
    - 4) Maintenance Instructions and Test Procedures
    - 5) Alignment and Operational Procedures
3. Electrical
- a. Analog Inputs
    - 1) Voltage and Current Ranges: As specified for each signal
    - 2) Input Impedance:  $50\Omega \pm 5\%$ , DC to 5 MHz minimum

3) Input Protection and Overload Recovery: Provided

b. Analog Outputs

1) Voltage and Current Ranges: As specified for each signal

2) Internal Impedance:  $50\Omega \pm 5\%$ , DC to 10 MHz

3) Short-circuit, Overload, and Overvoltage Protection:  
Provided

c. Logic Signals

1) An open-circuit (disconnected) input will be the same as a logic "0"

2) Short-circuit, Overload, and Overvoltage Protection:  
Provided

3) Computer/Logic Signals: Compatible with computer (Unit 6/ Unit 5) interface requirements

4) All other logic signals: TTL compatible

a) Logic "0": 0 to +0.25 volts, nominal  
-0.2 to +0.4 volts, maximum range

b) Logic "1": +3 to +4 volts, nominal  
+2.4 to +5 volts, maximum range

5) Each of the Units, 1 through 4, will provide a logic output that is a logic "1" when that unit's power is ON

d. Power

1) Each unit will provide all the power supplies necessary for its operation

2) Each unit will accept single-phase, 105 to 130 volts rms, 50 to 60 Hz input power. Step transients of 5% within the voltage range will not affect the operation of any unit

## Unit Specifications

All units must meet the foregoing general specifications, plus the following unit-unique specifications.

1. Signal Source: The signal source will provide an analog signal that is compatible with lowpass filter input requirements
2. Adjustable Lowpass Filter
  - a. Input Characteristics
    - 1) Maximum Input Amplitude: 3 volts rms (into 50 $\Omega$ )
    - 2) Maximum DC Component
      - a) Direct-Coupled Input: Combined ac plus dc should not exceed 4.3 volts (peak)
      - b) AC-Coupled Input: 50 volts
  - b. Output Characteristics
    - 1) Maximum Output Voltage: 3 volts rms (into 50 $\Omega$ ) up to 4.5 MHz
    - 2) Maximum Output Current:  $\pm$  85 ma. (peak)
  - c. Frequency Range: DC to 4.5 MHz, with thirteen switch-selectable passband cutoff ( $f_c$ ) and stopband threshold ( $f_t = 2 f_c$ ) breakpoint frequency pairs (See Table 2-7)
    - 1) Passband cutoff breakpoint frequencies ( $f_c$ ): 1.25 KHz, 2.5 KHz, 5 KHz, 10 KHz, 20 KHz, 40 KHz, 80 KHz, 160 KHz, 320 KHz, 625 KHz, 1.25 MHz, 2.5 MHz, and 4.5 MHz\*.
    - 2) Stopband threshold breakpoint frequencies ( $f_t$ ): 2.5 KHz, 5 KHz, 10 KHz, 20 KHz, 40 KHz, 80 KHz, 160 KHz, 320 KHz, 680 KHz, 1.25 MHz, 2.5 MHz, 5 MHz, and 5 MHz\*.

\*At the  $f_c = 4.5$  MHz filter setting (corresponding to a 10 MHz input sampling rate), the stopband threshold breakpoint is at 5 MHz (not 9 MHz). The filter must provide sufficient rolloff above 4.5 MHz so that the net filtered signal power at the filter output is less than -70 db (relative) at 5 MHz and above. For a 70 db/octave filter rolloff, the input power must be down to less than -60 db at 5 MHz and above. Otherwise, some degree of aliasing will be present in data sampled at the maximum 10 MHz rate.

- 3) AC-Coupled Input: 20 Hz (high-pass) cutoff breakpoint frequency ( $f_{hp}$ )
- d. Breakpoint Frequency Calibration Accuracy
  - 1)  $f_{hp} = 20 \text{ Hz} \pm 5\%$
  - 2)  $f_c = \text{selected value} \pm 5\%$
  - 3)  $f_t = 2_{fc} \text{ (or 5 MHz)} \pm 5\%$
- e. Response Characteristics (See Figure 2-17)
  - 1) AC-Coupled Input DC attenuation: Greater than 70 dB
  - 2) Passband (DC or 20 Hz to selected cutoff  $f_c$ ): +0, -0.5 dB (relative)
  - 3) Attenuation slope ( $f_c$  to  $f_t$ ): 70 dB/octave equivalent rolloff
  - 4) Stopband Attenuation ( $f_t$  and above): Greater than 70 dB
- f. Insertion Loss
  - 1) Less than 6 dB for all cutoff frequency settings
  - 2) Stability: Less than  $\pm 0.002$  db for 10 minutes at constant temperature
  - 3) Temperature Coefficient: Less than  $\pm 0.01$  dB per degree C
- g. Hum and Noise: Less than 100  $\mu$ volts rms
- h. Output DC Level Stability: Less than  $\pm 2$  mvolts per degree C
- i. Controls
  - 1) AC/Direct-Coupled Selection Switch (2 positions)
  - 2) Cutoff Frequency Selection Switch (13 positions)
  - 3) Power ON/OFF Switch (2 positions)
- j. Indicators: Power ON

k. Signal Connectors

- 1) Analog Input
- 2) Analog Output
- 3) Power ON (logic level)
- 4) Remote Programming (for Switch 2)

3. Adjustable Scaling Amplifier

- a. Amplifier Type: Direct and AC-Coupled, Variable Gain
- b. Input Range:  $\pm 10$  mvolts minimum to  $\pm 5$  volts maximum (peak-to-peak into  $50\Omega$ )
- c. Output Characteristics
  - 1) Output Voltage: Adjusted to  $\pm 5$  volts (p-p into  $50\Omega$ )
  - 2) Maximum Output Current:  $\pm 100$  ma. (peak)
- d. Frequency Response
  - 1) Direct-Coupled:  $\pm 0.002$  dB, DC to 4.5 MHz
  - 2) AC-Coupled:  $\pm 0.002$  db, 20 Hz to 4.5 MHz
- e. Gain Characteristics
  - 1) Selection: Continuously variable from 1 to 500
  - 2) Accuracy: Adjusted while visually observing output signal with oscilloscope and/or peak-reading volt meter or other suitable device
  - 3) Stability: With constant input level, output level varies less than  $\pm 5$  m volts ( $\pm 10$  m volts peak-to-peak) for 10 minutes at constant temperature
  - 4) Temperature Coefficient: With constant input level, output level varies less than  $\pm 5$  m volts ( $\pm 10$  m volts peak-to-peak) per degree C



- 5) Trim: Permits adjustment of output level to  $\pm 5$  volts (peak-to-peak) to within  $\pm 5$  m volts ( $\pm 10$  m volts peak-to-peak), with 2 m volts resolution or better
- f. DC Linearity: Maximum deviation of  $\pm 5$  m volts
- g. Zero Characteristics
  - 1) Stability: Less than  $\pm 5$  m volts for 10 minutes at constant temperature
  - 2) Temperature Coefficient: Less than  $\pm 5$  m volts per degree C
  - 3) Trim: 2 m volts or better resolution for zero offset adjustment
  - 4) Shorted input provided for adjusting zero offset
- h. Hum and Noise: Less than 100  $\mu$ volts rms
- i. Controls
  - 1) AC/GND (Shorted Input)/Direct-Coupled Selection Switch (3 positions)
  - 2) Coarse Gain Adjust
  - 3) Fine Gain Adjust
  - 4) Zero Offset Adjust
  - 5) Power ON/OFF Switch (2 positions)
- j. Indicators: Power ON
- k. Signal Connectors
  - 1) Analog Input
  - 2) Analog Output
  - 3) Power ON (Logic Level)
  - 4) Remote Programming (for adjustments 2 and/or 3)

#### 4. A/D Converter

##### a. Analog Input

- 1) Input Range:  $\pm 5$  volts
- 2) Input Bandwidth: DC to 10 MHz

##### b. Conversion Characteristics

- 1) Resolution: 9 bits (8 bits plus sign)
- 2) Sampling Rate: DC to 10 MHz
- 3) Aperture Time: 200 psec (0.2 n sec) or less
- 4) Throughout Conversion Time:\* Less than 100 n sec
- 5) Accuracy:  $\pm 0.05\% \pm 1/2$  LSB (least significant bit)

##### c. Convert Command (Command to Convert) Pulse

- 1) TTL logic compatible, positive-going (0"  $\rightarrow$  "1")
- 2) Pulse Width: 15 n sec. minimum to 30 n sec. maximum
- 3) Rise Time: Less than 10 n sec., 10% to 90%

##### d. EOC (End-of-Conversion or Data Ready) Pulse

- 1) TTL logic compatible, positive-going ("0"  $\rightarrow$  "1")
- 2) Pulse Width: 15 to 30 n sec
- 3) Rise Time: Less than 10 n sec

##### e. Digital Outputs

###### 1) Parallel Straight Binary Output Code

- |    |   |                          |
|----|---|--------------------------|
| a) | $+ 4.98 \text{ volts} \leq \text{Input}$          | $\Rightarrow 1111111111$ |
| b) | $0 \leq \text{Input} \leq + 19.5 \text{ m volts}$ | $\Rightarrow 100000000$  |
| c) | $-19.5 \text{ m volts} \leq \text{Input} < 0$     | $\Rightarrow 011111111$  |
| d) | $\text{Input} \leq - 4.98 \text{ volts}$          | $\Rightarrow 000000000$  |

\*From the beginning of the "command-to-convert" pulse to the beginning of the "end-of-conversion" pulse.

- 2) Output Skew: Less than 5 n sec.
- 3) TTL compatible
- f. Controls
  - 1) Power ON/OFF Switch (2 positions)
  - 2) TEST/OPERATE Switch (2 positions)
- g. Indicators
  - 1) Nine each: Data Output (one for each bit in output data word)
  - 2) Power ON
- h. Signal Connectors
  - 1) Analog Input
  - 2) Convert Command
  - 3) EOC
  - 4) Nine each: Output Data Word
- 5. Control Logic and Data Buffer
  - a. Provides operational functions as outlined in discussions of Figures 2-14, 2-18, and 2-19.
  - b. Input (Logic) Signals
    - 1) Four each: Power ON (Assy. 5A2): One each from Units 1 through 4
    - 2) Interrupt Enable (IE) (Assy. 5A2): From Unit 6\*
    - 3) Input Acknowledge (IA) (Assy. 5A2): From Unit 6\*
    - 4) External Start (Assy. 5A3A1): From Unit 7
    - 5) End-of-Conversion (EOC) (Assy. 5A3A2): From Unit 4
    - 6) Nine each: Digital Sample Word (Assy. 5A5): From Unit 4
    - 7) Remote Programming (for Switches 1 through 7)

\*Signal shapes, timing, connector pin assignments, etc. as specified in Computer Interface Design Manual.

c. Output (Logic) Signals

- 1) Interrupt (INT) (Assy. 5A2): To Unit 6\*
- 2) Convert (Command-to-Convert) (Assy. 5A3A2): To Unit 4
- 3) Input Data Request (IDR) (Assy. 5A4): To Unit 6\*
- 4) 29 each: Packed Data Word (Assy. 5A5): To Unit 6\*
- 5) Test Jack Signals: External and internal signals as required

d. Controls

- 1) Rate Select Switch (Assy. 5A1) (3 pole, 12 positions)
- 2) Reset Select Switch (Assy. 5A2) (2 positions)
- 3) Reset Switch (Assy. 5A2) (momentary bushbutton)
- 4) Start Select Switch (Assy. 5A3A1) (2 positions)
- 5) Start Switch (Assy. 5A3A1) (momentary pushbutton)
- 6) Clock Select Switch (Assy. 5A3A2) (2 positions)
- 7) Step Switch (Assy. 5A3A2) (momentary pushbutton)
- 8) Power ON/OFF Switch (2 positions)

e. Indicators

- 1) Hardware Power ON (Assy. 5A2)
- 2) Computer Ready (Assy. 5A3A1)
- 3) System Recycle (Assy. 5A3A1)
- 4) System Ready (Assy. 5A3A1)
- 5) Acquiring Data (Assy. 5A3A1)
- 6) Processing Data (Assy. 5A3A1)
- 7) Rate Too High For Converter (Assy. 5A5)

\*Signal shapes, timing, connector pin assignments, etc. as specified in Computer Interface Design Manual.

8) Rate Too High For Computer (Assy. 5A5)

9) Power ON

f. Signal Connectors: As specified in b & c above.

6. Computer - Data Acquisition Software Program

- a. The required data acquisition program is shown as a flow diagram in Figure B-1. To facilitate understanding of the overall system function, the diagram is expanded to include manual operations, an equivalent flow diagram of the control logic (Unit 5), and the interface signals between Units 5 and 6. The diagramming of the hardware is for reference only and does not constitute a specification of the hardware.
- b. Referring to Figure B-1, Sheet 1, after the hardware has been configured (Steps HA through HB), the software program is loaded and initialized. At Step SA, the parametric information for a particular data case is read-in from cards (or other suitable input device). This and other information is printed on the line printer (or other suitable output device), to provide a permanent record of the results of the data case being run.
- c. On Sheet 2, the computer activates the INTERRUPT ENABLE (IE) signal (to "inform" the hardware that the computer is ready to initiate a data acquisition sequence) and starts the runout or "watchdog" timer. At Step SB, if no interrupt is received by the time the runout expires, an error printout occurs. The two conditions that can lead to this error message are: One or more of the hardware units 1 through 5 are not on, or MANUAL RESET has been selected on Unit 5 and the RESET push-button has not yet been activated.
- d. Once an interrupt has been received from Unit 5 (Step I2a), the software disarms responses to further interrupts from Unit 5, disables (shuts-off) the runout timer, and initializes

DATA ACQUISITION HARDWARE

DATA ACQUISITION SOFTWARE

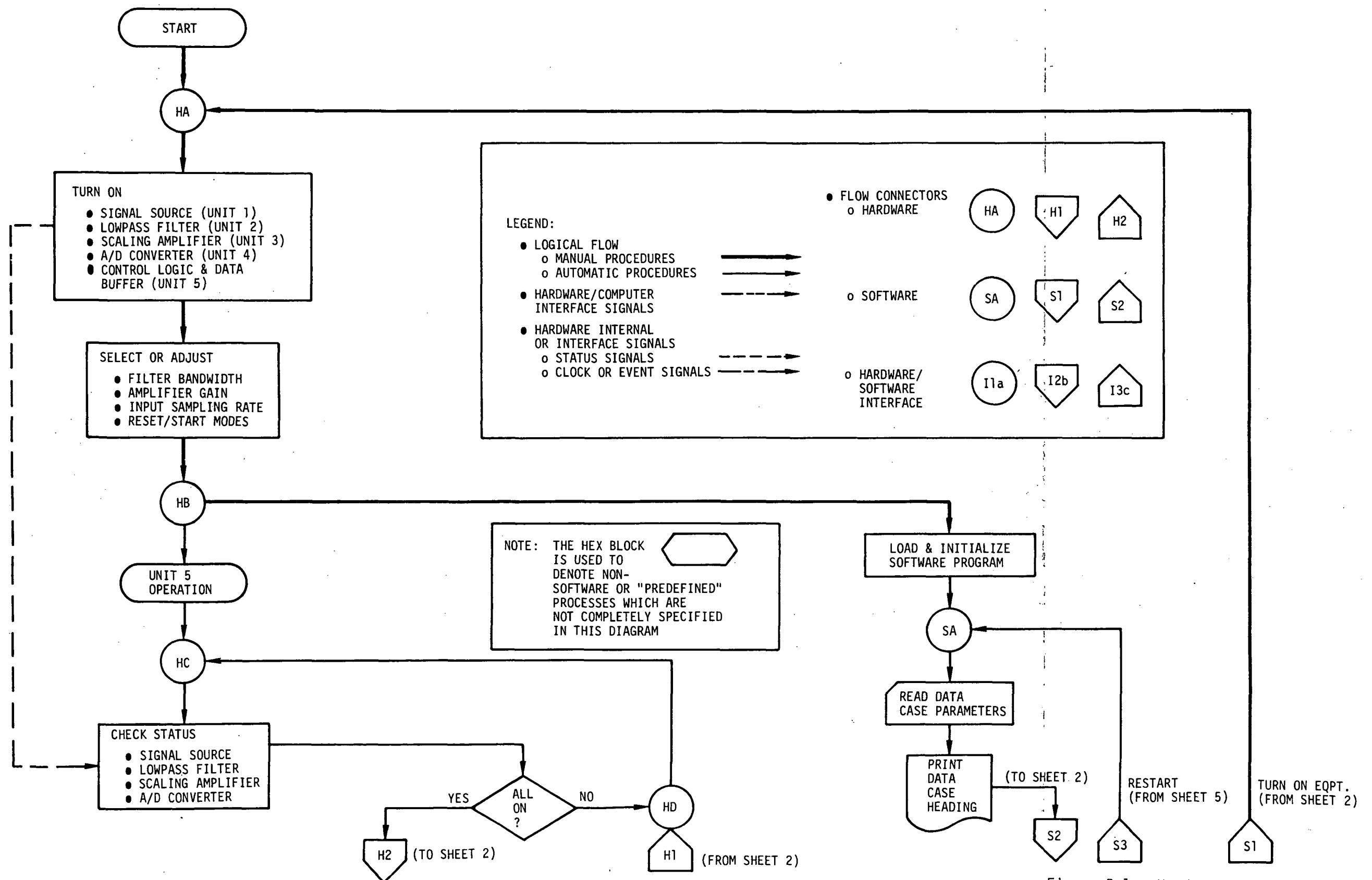


Figure B-1. Hardware/Software Flow Diagram (Sheet 1 of 5)

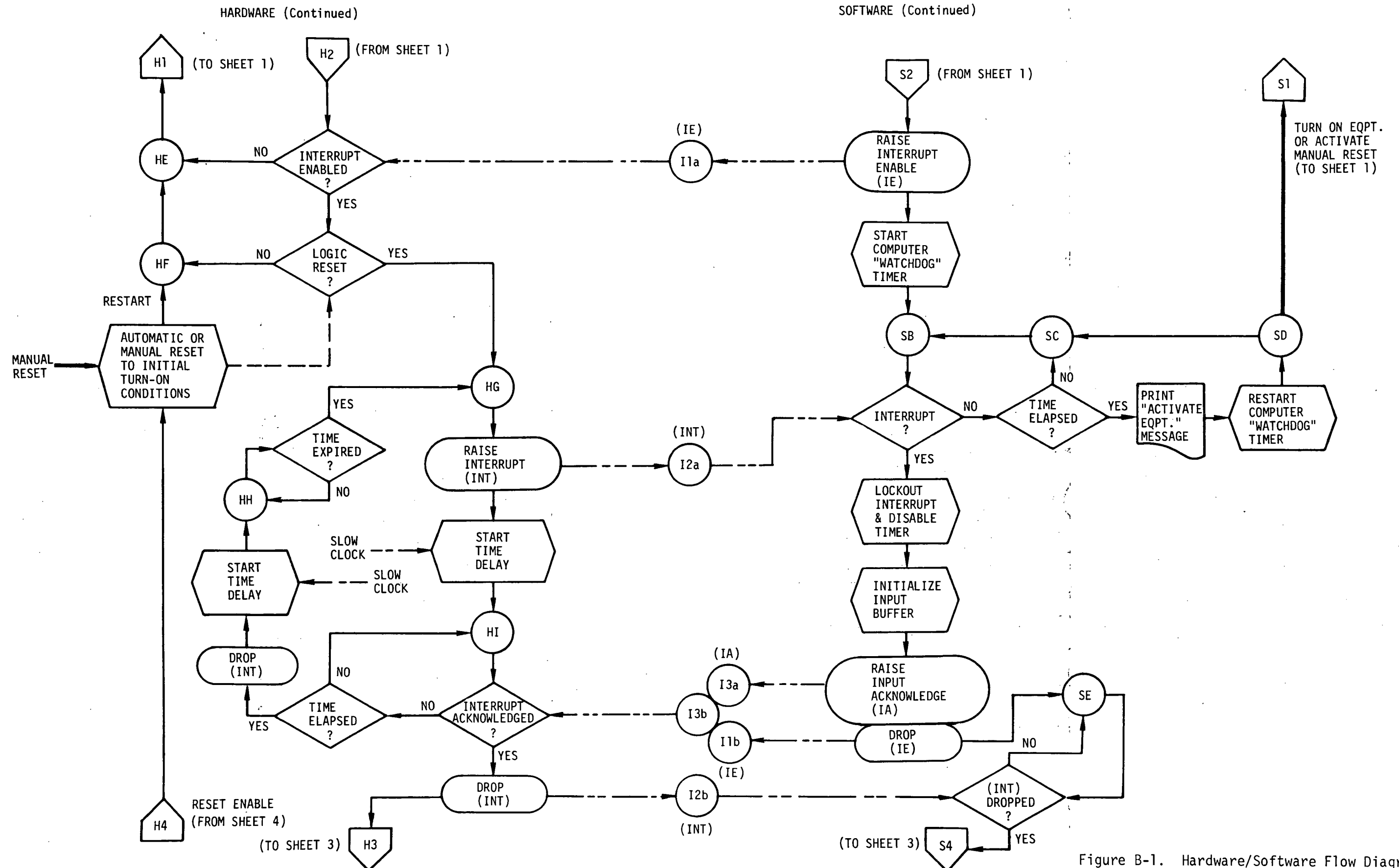


Figure B-1. Hardware/Software Flow Diagram  
(Sheet 2 of 5)

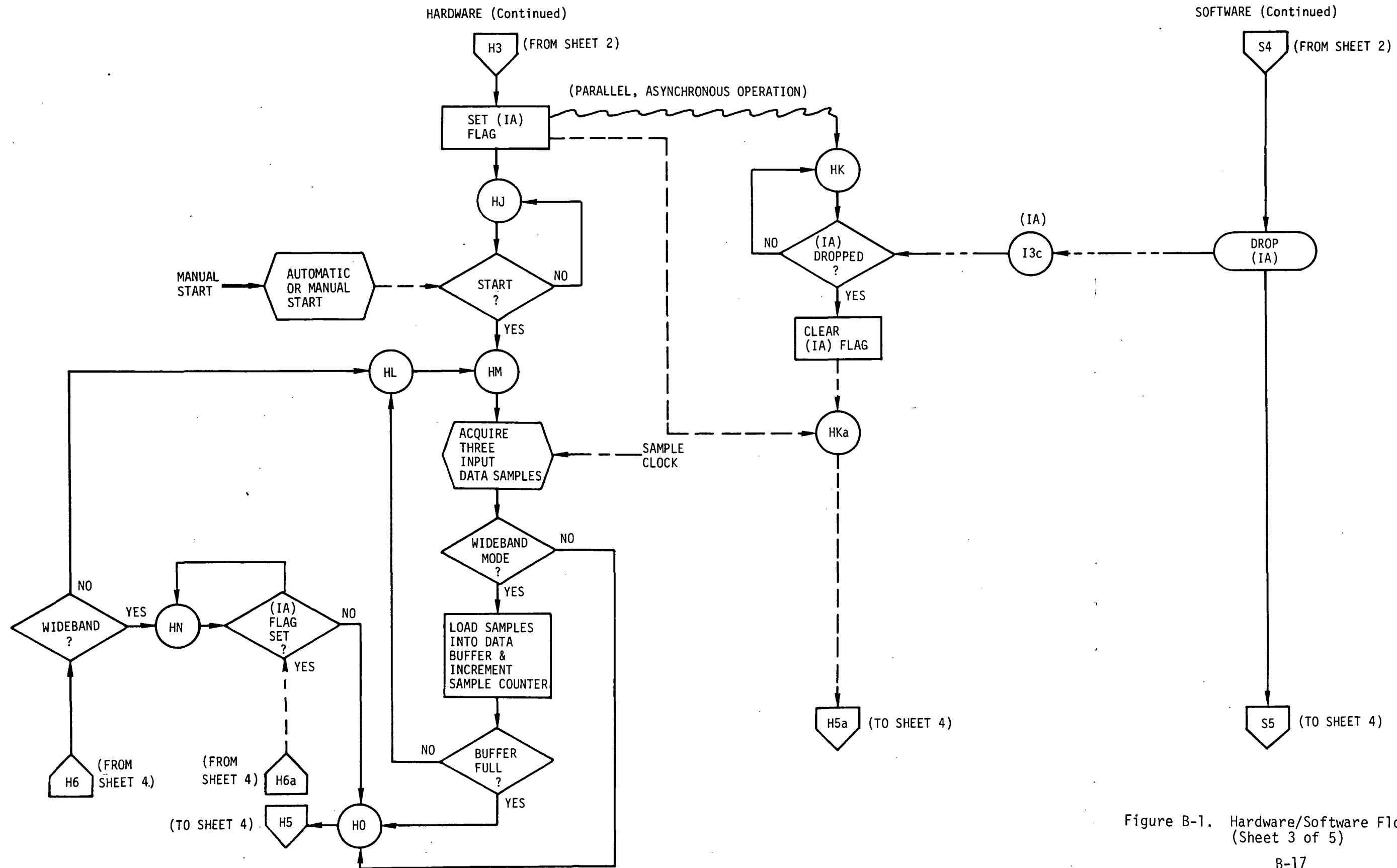
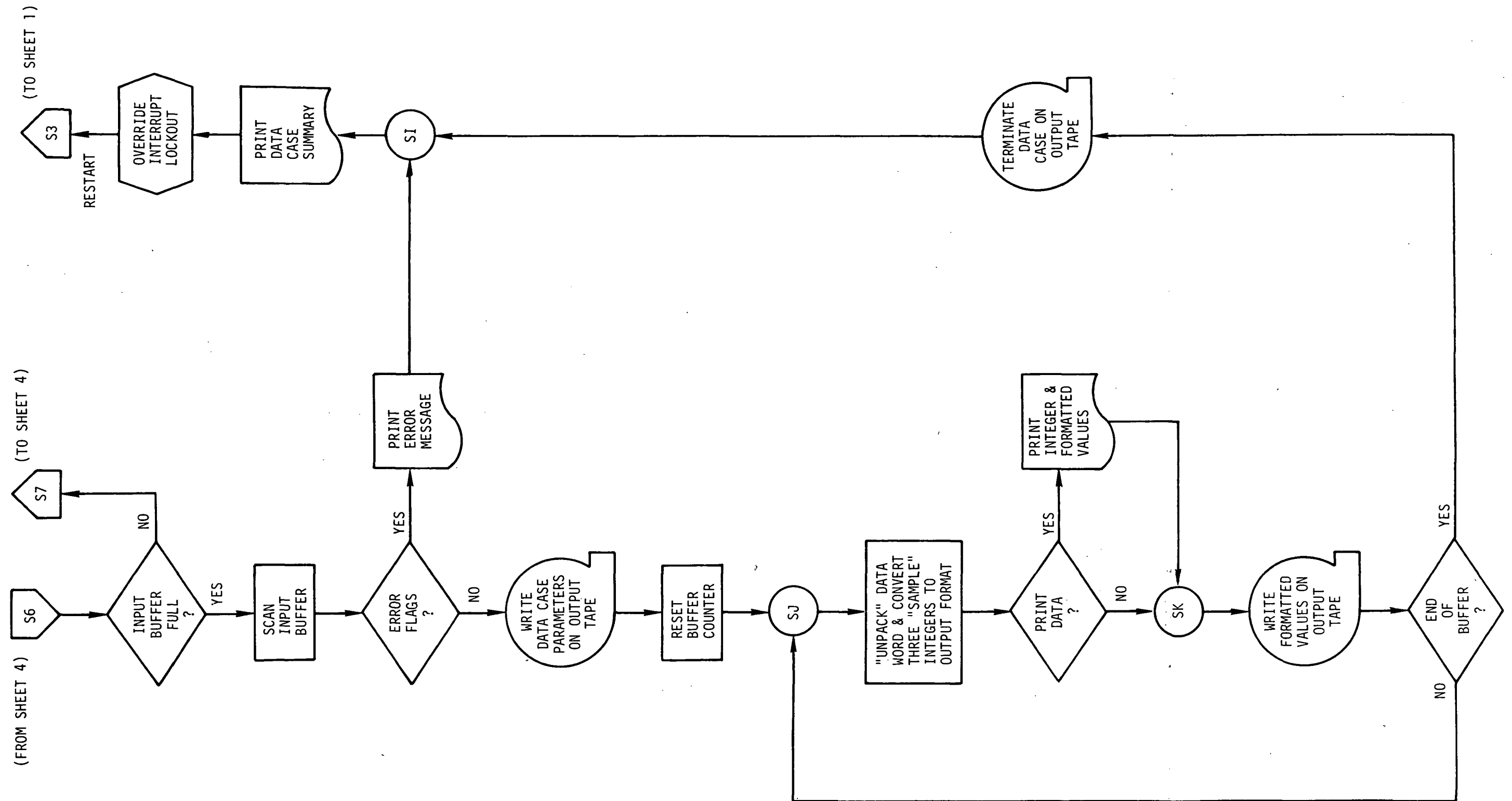


Figure B-1. Hardware/Software Flow Diagram (Sheet 3 of 5)



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Figure B-1. Hardware/Software Flow Diagram  
(Sheet 5 of 5)

the input buffer according to the number of data samples to be acquired, as determined by the data input at Step SA. When initialization of the input buffer is complete, the computer simultaneously raises the INPUT ACKNOWLEDGE (IA) signal and drops the (IE) signal. This combined event signals an interrupt acknowledge to Unit 5.

- e. While Unit 5 is waiting for one of its interrupts to be acknowledged, it periodically pulses the INTERRUPT (INT) signal on and off.\* Once an interrupt acknowledge is received, no further interrupts are activated until after the system has recycled to the next data case.
- f. After dropping the (INT) signal, Unit 5 enters the ready state (Step HJ, Sheet 3). Both the hardware and the software wait for the start event to occur, the hardware waiting at Step HJ and the software at Step SF (Sheet 4).
- g. After starting, Unit 5 enters the data acquisition mode, acquiring data samples from the A/D converter in groups of three. If operating in the wideband configuration, all data samples are stored in the Unit 5 data buffer before any of the data is transferred to the computer. In the narrowband configuration, data is transferred to the computer after each group of three input samples have been acquired.
- h. At Step H5, Sheet 4, three-sample words are loaded into the Unit 5 final output buffer and placed on the input data lines to the computer. If the (IA) signal is not active [(IA) Flag cleared), Unit 5 raises the INPUT DATA REQUEST (IDR) signal, sets the (IA) Flag, and cycles back to output the next set of three input samples (Step H6).

---

\*If the computer cannot operate with pulsed interrupts, the interrupt signal will remain "set" until it is "acknowledged".

- i. Upon receipt of the (IDR) signal, the computer reads (at its convenience) the input data word, stores it in the computer input buffer, and activates the INPUT ACKNOWLEDGE (IA) signal. The (IA) is dropped after Unit 5 drops the (IDR); Unit 5 clears the (IA) Flag as soon as (IA) is dropped.
- j. At Step H6, Sheet 3, narrowband operation continues with the acquisition of three more input samples. Wideband operation continues with the readout of the next data word in the Unit 5 data buffer; "wideband" readout does not occur until after the previous data word has been acknowledged.
- k. At Step HPa, Sheet 4, after a new output word has been placed on the computer input lines, Unit 5 sets an error flag in the data word if the (IA) flag has not yet been cleared. Effectively operational only for the narrowband configuration, this error flag indicates that the narrowband input sampling is occurring faster than the computer can read input data. This event is unlikely, since the maximum transfer rate in this case is only 6.7 KHz. Whenever an (IA) error occurs, the current output word is aborted, and Unit 5 recycles for the next data read-out.
- e. At Step S6, Sheet 5, the software loops back to Step SF, Sheet 4, loading a complete set of input data words into the computer input buffer. After the last data word has been loaded, the software begins processing the data. Unit 5 senses this condition at Step HR, Sheet 4: When no (IA) has been received by the time the "SLOW CLOCK" time delay has expired, the then currently active (IDR) is dropped, and Unit 5 recycles back to Step H4, Sheet 2. Unit 5 is then ready for a reset event, either manual or automatic (when the computer once again raises the (IE) signal).

- m. Referring to Sheet 5, once the computer input buffer has been filled, the software scans the error flag bits in each data word in the buffer until it finds one that is set. If one is found, all of the rest will be set, so the software aborts further processing, prints an error message, and recycles to the next data case.\*
- n. If no error flags are found in the input data, the software writes identifying information on the output tape and processes the contents of the input data buffer for output on the tape. Since the input samples have been packed three to a word, the software first strips out the three 9-bit integers. This can be accomplished through the use of bit-masking or word-shifting instructions. Next the software converts these integers to the (input) format required by the spectral analysis program. The integers range from 0 (for a maximum negative input signal) to 511 (for a maximum positive input signal), with a slightly greater than zero input signal being encoded as 256 and a slightly less than zero input signal being encoded as 255. The quickest procedure for converting the integers to the desired output format is to pre-store the possible output values in a table that is 512 entries long. The acquired data sample integers can then be used as the subscripts in a simple table lookup.\*\*

\*As an option, the software could be written to automatically retry an aborted input sample data case, since this is such an unlikely event.

\*\*For example, if the inputs to the spectral analysis program were to be in the range  $\pm 1.0$ , entry #0 would be  $-1.0$ , entry #1:  $-0.99609375$ , ..., entry #255:  $-0.00390625$ , entry #256:  $+0.00390625$ , ..., entry #510:  $+0.99609375$ , and entry #511:  $+1.0$ . Using mid-interval values, entry #0 would be  $-0.998046875$ , entry #1:  $-0.994140625$ , ..., entry #255:  $-0.001953125$ , etc. This latter format is preferred, since the spacing between consecutive entries is uniform (at  $0.00390625$ ). With the former format, all entries except #255 & 256 are separated by  $0.00390625$ , but #255 & 256 are separated by  $0.0078125$ .

- o. If the print option has been exercised, the software prints both the integer and formatted values, in addition to writing the formatted values on the output tape. Once all values have been output on the tape, the software terminates the data case (e.g., writing an end-of-file on the tape and printing a summary of the data case) and recycles to the next data case.

## 7. (Optional) Oscilloscope and/or Peak-Reading Voltmeter

Whether or not an oscilloscope, peak-reading voltmeter, or other suitable devices are used with the data acquisition system is at the user's discretion. However, there are two considerations which will enable maximum utilization of the system.

### a. Input Signal Amplitude Normalization

- 1) The A/D converter (Unit 4) has a  $\pm 5$  volts input dynamic range, divided with 9-bit resolution into 512 intervals of 0.01953125 volts each.
- 2) The scaling amplifier (Unit 3) output can be adjusted to  $\pm 5$  volts (peak-to-peak)  $\pm 5$  mvolts ( $\pm 10$  m volts peak-to-peak), with 2 mvolts resolution or better.
- 3) Whatever device is used for monitoring the Unit 3 output level while making the Unit 3 gain adjustment should be capable of resolving voltages in the range  $\pm 5$  volts to within  $\pm 5$  mvolts or better.

### b. "Start Conversions" Triggering

- 1) The control logic (Unit 5) has a provision for manual or automatic starting of the input data sampling (Assy. 5A3A1).
- 2) With a repetitive or predefined aperiodic input signal, the trigger output of an oscilloscope time base or other suitable triggering device could be used to provide the required external "START" pulse or level transition. This signal should be level-shifted to be TTL-compatible.

## 5. REFERENCES

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